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EXAR

APPLICATIONS DATA BOOK

First in Quality... First in Service • Custom, Semi-custom and Standard IC's

Introduction

This Data Book contains a comprehensive collection of application notes and technical articles, prepared by Exar's engineering staff. These articles cover the use and applications of Exar's broad line of monolithic IC products. The applications and design examples discussed cover a wide range of subjects, from FSK Modem design to electronic music synthesis. In each case, specific design examples are given to illustrate the use of the integrated circuit in that particular application or end product.

EXPERIENCE AND PRODUCTS

Exar's innovativeness, product quality and responsiveness to customer needs have been the key to its success. Exar today offers a broad line of linear and interface circuits. In the field of standard linear IC products, Exar has extended its circuit technological leadership into the areas of communications and control circuits. Today Exar has one of the most complete lines of IC oscillators, timing circuits and phase-locked loops in the industry. Exar also manufactures a large family of telecommunication circuits such as tone decoders, compandors, modulators, PCM repeaters and FSK Modem Circuits. In the field of industrial control circuits, Exar manufactures a broad line of quad and dual operational amplifiers,voltage regulators, radio-control and servo driver IC's, and power control circuits.

Exar's experience and expertise in the area of bipolar IC technology extends both into custom and standard IC products. In the area of custom IC's, Exar has designed, developed, and manufactured a wide range of full-custom monolithic circuits, particularly for applications in the areas of telecommunications, consumer electronics, and industrial controls.

In addition to the full-custom capability, Exar also offers a unique semi-custom IC development capability for low to medium-volume custom circuits. This semi-custom program, is intended for those customers seeking cost-effective solutions to reduce component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turnaround time of several weeks at a small fraction of the cost of a full-custom development program.

EXCELLENCE IN ENGINEERING

Exar quality starts in Engineering where highly qualified people are backed up with the advanced instruments and facilities needed for design and manufacture of custom, semi-custom and standard integrated circuits. Exar's engineering and facilities are geared to handle all three classes of IC design: (1) semi-custom design programs using Exar's bipolar and I^2L master chips; (2) full-custom IC design; (3) development and high-volume production of standard products.

Some of the challenging and complex development programs successfully completed by Exar include analog compandors and PCM repeaters for telecommunication, electronic fuel-injection, anti-skid braking systems and voltage regulators for automotive electronics, digital voltmeter circuits, 40-MHz frequency synthesizers, high-current and high-voltage display and relay driver ICs, and many others.

NEW TECHNOLOGIES

Through company sponsored research and development activities, Exar constantly stays abreast of all technology areas related to changing customer needs and requirements. Exar has recently completed development efforts in Integrated Injection Logic (I^2L) technology, which offers unique advantages in the area of low-power, high-density logic arrays. Exar has a complete design engineering group dedicated to this new technology, and is currently supplying over twenty different custom and semi-custom I^2L products.

FIRST IN QUALITY

From incoming inspection of all materials to the final test of the finished goods, Exar performs sample testing of each lot to ensure that every product meets Exar's high quality standards. Exar's manufacturing process is inspected or tested in accordance with its own stringent Quality Assurance Program, which is in compliance with MIL-Q-9858A. Additional special screening and testing can be negotiated to meet individual customer requirements.

Throughout the wafer fab and assembly process, the latest scientific instruments, such as scanning electron microscopes, are used for inspection, and modern automated equipment is used for wafer probe, AC, DC, and functional testing. Environmental and burn-in testing of finished products is also done in-house. For special environmental or high reliability burn-in tests outside testing laboratories are used to complement Exar's own extensive in-house facilities.

FIRST IN SERVICE

Exar has the ability and flexibility to serve the customer in a variety of ways from wafer fabrication to full parametric selection of assembled units for individual customer requirements. Special marking, special packaging and military screening are only a few of the service options available from Exar. We are certain that Exar's service is flexible enough to satisfy 99% of your needs. The company has a large staff of Applications Engineers to assist the customer in the use of the product and to handle any request, large or small.

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Overview of Exar's Application Notes

The following list gives a brief summary, and the description, of the subject material covered in each one of Exar's Application Notes included in this Data Book.

AN-01: Stable FSK Modems Featuring the XR-2206, XR-2207 and XR-2211
Design of stable full-duplex FSK modems is described using the XR-2206 or the XR-2207 as the modulator, and the XR-2211 as the demodulator with carrier-detection capability. Complete design examples are given for FSK modems covering mark/space frequencies from a few Hertz to 100 kHz.

AN-02: XR-C240 Monolithic PCM Repeater
The principle of operation of the XR-C240 monolithic regenerative repeater IC is described. Design examples and external connections of the circuit are discussed for applications in T-1 type 1.544 Megabit PCM telephone lines.

AN-03: Active Filter Design with IC Op Amps
This application note is intended to familiarize the filter designer with the fundamentals of active filter design, using monolithic IC op amps. It presents a table of transfer functions and network equations for high-pass, low-pass, band-pass and band-reject filters. Several design examples are given to illustrate the respective merits and limitations of various filter configurations. Particular emphasis is given to applications of programmable quad operational amplifiers, such as the XR-4202, as an active filter element in FSK Modems.

AN-04: XR-C277 Low-Voltage PCM Repeater IC
The design principles and the applications of the XR-C277 low-voltage (6.3 volt) regenerative PCM repeater are described. The monolithic IC contains all the basic functional blocks of a conventional PCM repeater, including the automatic line built-out section. Circuit connection diagrams and application examples are given for operation in 1.544 Megabit T-1 type PCM telephone systems.

AN-05: Tri-State FSK Modem Design Using XR-2207/XR-2211
Design of FSK modems with carrier detection and control capability are discussed. Such a "tri-state" modem uses a third carrier frequency for control functions, in addition to the normal "mark" and "space" frequencies used in conventional "bi-state" FSK systems. This carrier control feature allows each transmitter in a modem system to be automatically interrogated, one at a time, by a control processor, without interference from other modem transmitters within the system.

AN-06: Precision PLL System Using XR-2207/XR-2208
A two-chip versatile phase-locked loop system is described, using the XR-2207 oscillator as the VCO, and the XR-2208 multiplier as the phase detector. The resulting PLL system features 20 ppm/°C temperature stability. Design equations are given to tailor the circuit parameters to specific applications.

AN-07: Single-Chip Frequency Synthesizer Employing the XR-2240 (Reprinted in This Data Book)
The operation of the XR-2240 programmable/counter IC as a frequency synthesizer is described. The circuit can simultaneously multiply an input frequency by an integer modulus M, and divide it by a different modulus N+1. Thus, a wide range of non-integer output frequencies can be produced from a single input reference frequency.

AN-08: Dual-Tone Decoding with XR-567 and XR-2567
Application examples are given for simultaneous or sequential decoding of dual-tone control signals using either two XR-567 PLL tone decoders, or a single XR-2567 dual tone decoder. The examples include high-speed, narrow-band tone detection and Touch-Tone® decoding.

AN-09: Sinusoidal Output from XR-215 Monolithic PLL Circuit
A simple circuit technique is described to convert the VCO output of the XR-215 into a low-distortion sinewave. The external sinewave-shaping circuit is obtained using the XR-C101 monolithic NPN transistor array.

AN-10: XR-C262 High-Performance PCM Repeater
The design principle and the electrical characteristics of the XR-C262 high-performance PCM repeater IC are described. The circuit contains all the active components necessary for a regenerative PCM repeater system and operates with a single 6.8 volt power supply. Circuit connection and application examples are given for its use in 1.5 Megabit or 2 Megabit PCM systems.

AN-11: A Universal Sinewave Converter Using the XR-2208 and XR-2211
A circuit technique is described which can convert *any* periodic waveform into a low-distortion sinewave. The circuit operation is completely independent of input waveform amplitude and frequency as long as the input signal is periodic, and can operate over a frequency range of 1 Hz to over 100 kHz.

AN 12: Designing High Frequency Phase-Locked Loop Carrier-Detector Circuits
A design technique is described for high frequency tone or carrier detection. The two-chip circuit uses either the XR-210 or the XR-215 PLL circuit, in conjunction with the XR-2228 multiplier/detector, and can operate with carrier frequencies up to 20 MHz.

AN-13: Frequency Selective AM Detection Using Monolithic Phase-Locked Loops
The fundamentals of synchronous AM detection techniques are reviewed. The application of monolithic PLL circuits for frequency-selective AM detection is discussed. Several design examples are given, both for low- and high-frequency demodulation applications, using the XR-2212 or the XR-215 PLL circuits, in conjunction with the XR-2228 modulator/detector integrated circuit.

AN-14: A Complete Function Generator System Using the XR-2206
A laboratory quality self-contained function generator system is described, using the XR-2206 waveform generator IC. Complete circuit connection diagram, parts list and assembly instructions are given for a DC to 100 kHz self-contained function generator system with AM/FM capability and triangle, sine and square wave output.

AN-15: An Electronic Music Synthesizer Using the XR-2207 and the XR-2240 (Reprinted in This Data Book)
Design of a simple, low-cost "music synthesizer" system is described. The electronic music synthesizer is comprised of the XR-2207 voltage-controlled oscillator IC which is driven by the pseudo-random binary pulse pattern generated by the XR-2240 counter/timer circuit.

AN-16: Semi-Custom LSI Design with I^2L Gate Arrays
A unique design approach to developing complex LSI systems is described using XR-300 and XR-500 I^2L gate arrays. This technique greatly reduces the design and tooling cost and the prototype fabrication cycle associated with the conventional full-custom IC development cycle; and thus makes custom ICs economically feasible even at low production volumes.

AN-17: XR-C409 Monolithic I^2L Test Circuit
A monolithic test circuit has been developed for evaluation of speed and performance capabilities of Exar's Integrated Injection Logic (I^2L) technology. This test circuit, designated the XR-C409, is intended to familiarize the I^2L user and the system designer with some of the performance features of I^2L such as its frequency capability and power-speed tradeoffs.

Additional Technical Literature

As a companion set to this Applications Data Book, Exar's technical staff and applications engineers have prepared a series of additional Data Books which cover some of the key features and applications of Exar's other IC products. These Data Books also present a number of tutorial articles on the fundamentals of such important IC products as timers, phase-locked loops, and voltage-controlled oscillators. These books are available directly from your Exar sales or technical representative.

A brief description of each of these data books is given below:

TIMER DATA BOOK:

This data book provides a collection of technical articles and application information on monolithic timer IC products. Also included are the data sheets and the detailed electrical specifications of all of Exar's timer circuits, including the programmable timer/counters, micropower and long-delay timers. (48 pages)

FUNCTION GENERATOR DATA BOOK:

This comprehensive data book contains a number of technical articles and application notes on monolithic voltage-controlled oscillator (VCO) and function generator IC products. In addition, the data sheets and technical specifications of Exar's monolithic VCO's and function generators are given. (50 pages)

LINEAR AND DIGITAL SEMI-CUSTOM DESIGN BROCHURE:

This brochure contains a detailed description of Exar's unique bipolar and integrated injection logic (I^2L) semi-custom design technology. Economic advantages of the semi-custom designs are discussed and economic guidelines are given for choosing the most cost-effective solution to a custom IC requirement. In addition, this brochure provides technical information on Exar's Master Chips and IC Design Kits. (36 pages)

OPERATIONAL AMPLIFIER DATA BOOK:

This book contains a collection of technical articles on the fundamentals of monolithic IC op-amps. Some of the basic op-amp circuits are given, and the applications of IC op-amps in active filter design are discussed. The book also contains a complete set of electricl specifications in Exar's bipolar and BIFET op-amp products. (60 pages)

PHASE-LOCKED LOOP DATA BOOK:

This data book covers the fundamentals of design and applications of monolithic phase-locked loop (PLL) circuits. A long list of PLL applications are illustrated covering FM demodulation, frequency synthesis, FSK and tone detection. Particular emphasis is given to application of PLL circuits in data interface and communication systems such as FSK modems. This book also contains the data sheets and electrical specifications of all of Exar's PLL products. (74 pages)

Application Note AN-01

Stable FSK Modems Featuring the XR-2207, XR-2206 and XR-2211

INTRODUCTION

Frequency shift keying (FSK) is the most commonly used method for transmitting digital data over telecommunications links. In order to use FSK, a modulator-demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again.

This Applications Note describes the design of a modem using state-of-the-art Exar devices specifically intended for modem application. The devices featured are the XR-2206 and XR-2207 FSK modulators, and the XR-2211 FSK demodulator with carrier-detect capability. Because of the superior frequency stability (typically 20 ppm/°C) of these devices, a properly designed modem using them will be virtually free of the temperature and voltage-dependent drift problems associated with many other designs. In addition, the demodulator performance is independent of incoming signal strength variation over a 60 dB dynamic range. Because bias voltages are generated internally, the external parts count is much lower than in most other designs. The modem designs shown in this Applications Note can be used with mark and space frequencies anywhere from several Hertz to 100 kiloHertz.

THE XR-2206 FSK MODULATOR

FEATURES

- Typically 20 ppm/°C temperature stability
- Choice of 0.5% THD sinewave, triangle, or squarewave output
- Phase-continuous FSK output
- Inputs are TTL and C/MOS compatible
- Low power supply sensitivity (0.01%/V)
- Split or single supply operation
- Low external parts count

OPERATION

The XR-2206 is ideal for FSK applications requiring the spectral purity of a sinusoidal output waveform. It offers TTL and C/MOS compatibility, excellent frequency stability, and ease of application. The XR-2206 can typically provide a 3 volt p-p sinewave output. Total harmonic distortion can be trimmed to 0.5%. If left untrimmed, it is approximately 2.5%.

The circuit connection for the XR-2206 FSK Generator is shown in Figure 1. The data input is applied to pin 9. A high level signal selects the frequency $(1/R_6C_3)$ Hz; a low level signal selects the frequency $(1/R_7C_3)$ Hz, (resistors in ohms and capacitors in farads). For optimum stability, R_6 and R_7 should be within the range of 10 kΩ to 100 kΩ. The voltage applied to pin 9 should be selected to fall between ground and V+.

Note: Over and under voltage may damage the device.

Potentiometers R_8 and R_9 should be adjusted for minimum total harmonic distortion. In applications where minimal distortion is unnecessary, pins 15 and 16 may be left open-circuited and R_8 may be replaced by a fixed 200Ω resistor. In applications where a triangular output waveform is satisfactory, pins 13 thru 16 may be left open-circuited.

The output impedance at pin 2 is about 600Ω. In most applications, AC coupling of the output is recommended.

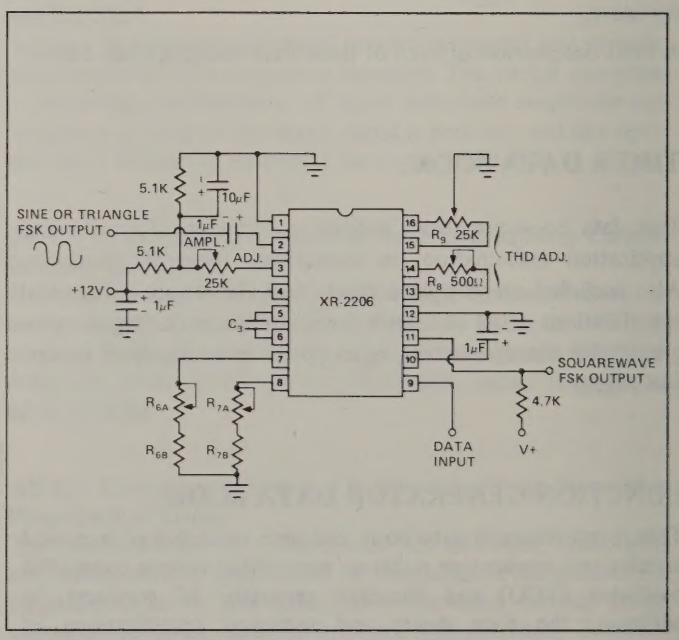


Figure 1. The XR-2206 Sinusoidal FSK Generator

THE XR-2207 FSK MODULATOR

FEATURES

- Typically 20 ppm/°C temperature stability
- Phase-continuous FSK output
- Provides both triangle and squarewave outputs
- Operates single-channel or two-channel multiplex
- Inputs are TTL and C/MOS compatible
- Split or single power supply operation
- Low power supply sensitivity (0.15%/V)
- Low external parts count

OPERATION

The XR-2207 is a stable FSK generator which is designed for those applications where only a triangle or squarewave output is required. It is capable of either single-channel or two-channel multiplex operation, and can be used easily with either split or single power supplies.

Figure 2 shows the XR-2207 using a single-supply and Figure 3 shows split-supply operation. When used as an FSK modulator pins 8 and 9 provide the digital inputs. When the 2207 is used with a split-supply, the threshold at these pins is approximately +2 volts, which is a level that is compatible with both TTL and C/MOS logic forms. When used with a single supply, the threshold is near mid-supply and is C/MOS compatible. Table 1 shows how to select the timing resistors R_1 thru R_4 to determine the output frequency based upon the logic levels applied to pins 8 and 9. For optimum stability, the values of R_1 and R_3 should be selected to fall between 10 kΩ and 100 kΩ.

With pin 8 grounded, pin 9 serves as the data input. A high level signal applied to pin 8 will disable the oscillator. When used in this manner, pin 8 of the XR-2207 serves as the channel select input. For two-channel multiplex operation, pins 4 and 5 should be connected as shown by the dotted lines. (For single channel operation, pins 4 and 5 should be left open-circuited.)

The XR-2207 provides two outputs; a squarewave at pin 13 and a trianglewave at pin 14. When used with a split-supply, the trianglewave peak-to-peak amplitude is equal to V– and the dc level is near ground. Direct coupling is usually used. With a single-supply, the peak-to-peak amplitude is approximately equal to ½V+, the DC level is at approximately mid-supply and AC coupling is usually necessary. In either case, the output impedance is typically 10Ω and is internally protected against short circuits.

The squarewave output has an NPN open-collector configuration. When connected as shown in Figure 2 or 3 this output voltage will swing between V+ and the voltage at pin 12.

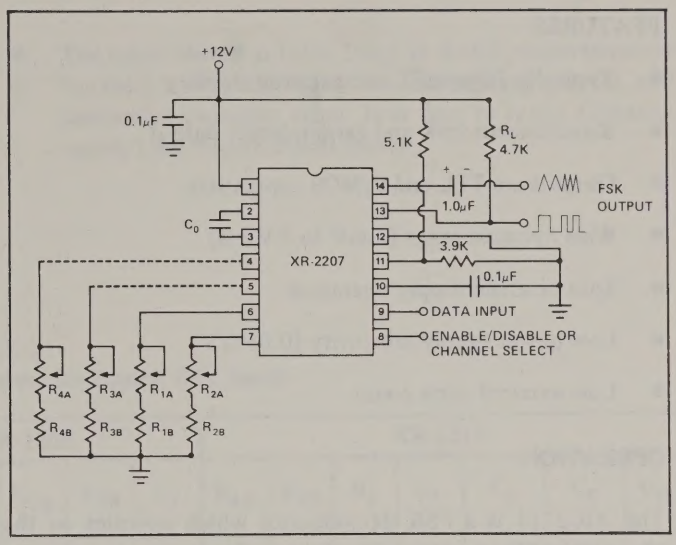


Figure 2. The XR-2207 FSK Modulator Single-Supply Operation

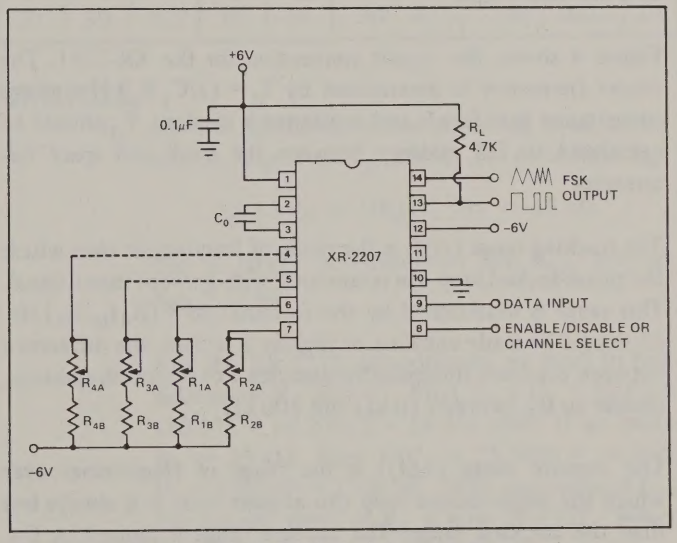


Figure 3. The XR-2207 FSK Modulator Split-Supply Operation

TABLE 1
XR-2207 FSK Input Control Logic

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pins 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pins 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

Units: Resistors – Ohms; Capacitors – Farads; Frequency – Hz

THE XR-221 FSK DEMODULATOR WITH CARRIER DETECT

FEATURES

- Typically 20 ppm/°C temperature stability
- Simultaneous FSK and carrier-detect output
- Outputs are TTL and C/MOS compatible
- Wide dynamic range (2 mV to 3 Vrms)
- Split or single supply operation
- Low power supply sensitivity (0.05%/V)
- Low external parts count

OPERATION

The XR-2211 is a FSK demodulator which operates on the phase-locked-loop principle. Its performance is virtually independent of input signal strength variations over the range of 2 mV to 3 Vrms.

Figure 4 shows the circuit connection for the XR-2211. The center frequency is determined by $f_0 = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. F_0 should be calculated to fall midway between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula: $\Delta f = (R_4 f_0/R_5)$ Hz. Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, choose an R_4 between 10 kΩ and 100 kΩ.

The capture range ($\pm\Delta f_c$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop filter time constant. In most modem applications, $\Delta f_c = (80\% - 99\%)\,\Delta f$.

The loop damping factor (ζ) determines the amount of overshoot, undershoot, or ringing present in the phase-locked loop's response to a step change in frequency. It is determined by $\zeta = \frac{1}{4}\sqrt{C_1/C_2}$. For most modem applications, choose $\zeta \approx \frac{1}{2}$.

The FSK output filter time constant (τ_F) removes chatter from the FSK output. The formula is: $\tau_F = R_F C_F$. Normally calculate τ_F to be approximately equal to [0.3/(baud rate)] seconds.

The lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510 kΩ, the minimum value of C_D can be determined by: $C_D\ (\mu f) \approx 16$/capture range in Hz.

Note: Excessive values of C_D will unnecessarily slow the lock-detect response time.

The XR-2211 has three NPN open collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, Pin 5 is the Q lock-detect output, which goes low when a carrier is detected, and Pin 6 is the $\overline{Q}$ lock detect output, which goes high when lock is detected. If pins 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied and will be "low" when no carrier is present.

If the lock-detect feature is not required, pins 3, 5 and 6 may be left open-circuited.

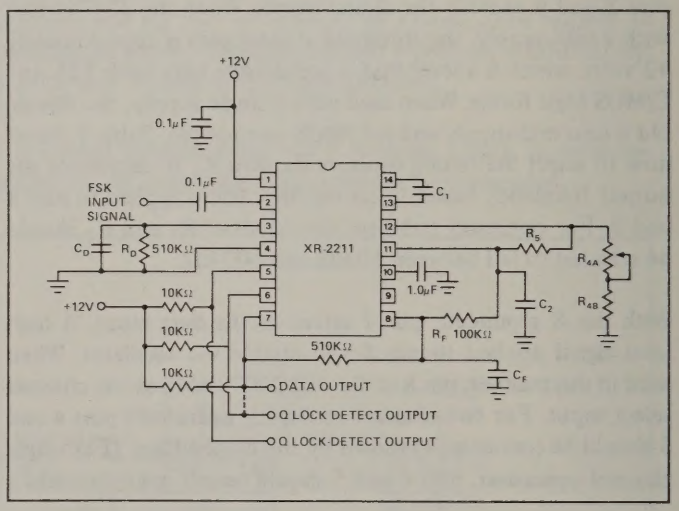


Figure 4. The XR-2211 FSK Demodulator with Carrier Detect

DESIGNING THE MODEM

Table 2 shows recommended component values for the three most commonly used FSK bands. In many instances, system constraints dictate the use of some non-standard FSK band. The XR-2206/XR-2207, XR-2211 combination is suitable for any range of frequencies from several Hertz to 100 kiloHertz.

Here are several guidelines to use when calculating non-standard frequencies:

- For maximum baud rate, choose the highest upper frequency that is consistent with the system bandwidth.
- The lower frequency must be at least 55% of the upper frequency. (Less than a 2:1 ratio)
- For minimum demodulated output pulsewidth jitter, select an FSK band whose mark and space frequencies are

both high compared to the baud rate. (i.e., for a 300 baud channel, mark and space frequencies of 2025 Hz and 2225 Hz would result in significantly less pulsewidth jitter than 300 Hz and 550 Hz).

- For any given pair of mark and space frequencies, there is a limit to the baud rate that can be achieved. When maximum spacing between the mark and space frequencies is used (where the ratio is close to 2:1) the relationship

$$\frac{\text{mark-space frequency difference (Hz)}}{\text{maximum data rate (baud)}} \geqslant 83\%$$

should be observed.

For narrower spacing, the minimum ratio should be about 67%.

- The values shown in Table 2 may be scaled proportionately for mark and space frequencies, maximum baud rate, and (inversely) capacitor value. It is best to retain (approximately) the resistor values shown.

TABLE 2
Recommended Component Values for Typical FSK Bands

FSK Band			XR-2207					XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{1A} R_{3A}	R_{1B} R_{3B}	R_{2A} R_{4A}	R_{2B} R_{4B}	C_0	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_{4A}	R_{4B}	R_5	C_1	C_2	C_F	C_D
300	1070	1270	10	20	100	100	.039	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
300	2025	2225	10	18	150	160	.022	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05
1200	1200	2200	20	30	20	36	.022	10	16	20	30	.022	10	18	30	.027	.01	.0022	.01

Units: Frequency – Hz; Resistors – kΩ; Capacitors – μF

DESIGN EXAMPLES

A. Design a modem to handle a 10 kilobaud data rate, using the minimum necessary bandwidth.

1. Frequency Calculation

Because we want to use the minimum possible bandwidth (lowest possible upper frequency) we will use a 55:100 frequency ratio. The frequency difference, or 45% of the upper frequency, will be 83% of 10,000. We therefore choose an upper frequency:

$$\frac{83 \times 10{,}000}{45} = 18.444 \text{ kHz} \approx 18.5 \text{ kHz}.$$

and the lower frequency:

$$0.55 \times 18.5 \text{ kHz} = 10.175 \text{ kHz}.$$

2. Component Selection

a. For the XR-2207 FSK modulator, set $R_1 \approx 30\,k\Omega$. Now, select a value of C_0 to generate 10.175 kHz with R_1:

$$10.175 \text{ kHz} = 1/(C_0 \times 30{,}000)\ ;\ C_0 = 3300 \text{ pF}.$$

To choose R_2:

$$18.500 \text{ kHz} - 10.175 \text{ kHz} = 8.325 \text{ kHz} = 1/C_0R_2\ ;\ R_2 = 36\,k\Omega.$$

A good choice would be to use 10 kΩ potentiometers for R_{1A} and R_{2A}, and to set $R_{1B} = 24\,k\Omega$ and $R_{2B} = 30\,k\Omega$.

b. For the XR-2206, we can make R_7 equal to R_1 and C_3 equal to C_0 above. To determine R_6:

$$18.5 \text{ kHz} = 1/R_6C_3\ ;\ R_6 = 16\,k\Omega.$$

Use a 10 kΩ potentiometer for R_{6A} and set $R_{6B} = 13\,k\Omega$.

c. For the XR-2211 demodulator, we need to first determine R_4 and C_1. First, $f_0 = (f_L + f_H)/2 = (10.175 + 18.500)/2 = 14.338$ kHz. If we make $R_4 = 25\,k\Omega$, then $1/(C_1 \times 25{,}000) = 14{,}338$; $C_1 = 2790\text{ pF} \approx 2700$ pF. With that value of C_1, the precise value of R_4 is now 25.8 kΩ. Select $R_{4B} = 18\,k\Omega$ and use a 10 kΩ for R_{4A}.

3. Frequency Component Selection

a. To calculate R_5, we first need our Δf, which is 18.500 – 10.175, or 8.325 kHz.

$$8325 = (25{,}800 \times 14{,}338)/R_5\ ;\ R_5 = 44.4\,k\Omega \approx 47\,k\Omega.$$

b. To determine C_2 use $\zeta = \frac{1}{2} = \frac{1}{4}\sqrt{C_1/C_2}$. Then, $C_2 = \frac{1}{4}\,C_1$; $C_2 = 670$ pF.

c. To select C_F, we use τ_F = [0.3/(baud rate)] seconds.

$$\tau_F = 0.3/10{,}000 = 30\ \mu\text{sec.}\ ;$$

with

$$R_F = 100\,k\Omega, C_F = 300 \text{ pF}.$$

4. Lock Range Selection

To select C_D, let us start with the actual lock range:

$$\Delta f = R_4 f_0 / R_5 \text{ Hz} = 7870 \text{ Hz}.$$

If we assume a capture range of 80%,

$$\Delta f_C = 6296 \text{ Hz};$$

therefore, our total capture range or $\pm\Delta f_C$ is 12,592 Hz. Our minimum value for C_D is (16/12,592) μf or 0.0013 μf.

5. Completed Circuit Example

See Figure 5.

B. Design a 3 kilobaud modem to operate with low output jitter. The bandwidth available is 13 kHz.

For this modem, we can take the values from 2 for the 300 baud modem operating at 1070 Hz and 1270 Hz, multiply our baud rate and mark and space frequencies by 10, and divide all capacitor values on the table by 10. Resistor values should be left as they are.

C. Design a 2 channel multiplex FSK modulator to operate at the following pairs of mark and space frequencies: 600 Hz and 900 Hz, and 1400 and 1700 Hz. (Each of these channels could handle about 400 baud.)

For this task, we will use the XR-2207. The only real consideration here is that, if possible, we want to keep the following resistances all between 10 kΩ and 100 kΩ: R_1, R_1/R_2, R_3 and R_3/R_4. The ratio between the maximum and minimum frequencies is less than 3:1, so we should have no trouble meeting this criterion. If we set our maximum frequency with an R of about 20 kΩ, we have: $1700 = 1/(C_0 \times 20{,}000)$; $C_0 = 0.029$ μf which is approximately equal to 0.033 μf.

Calculating R_1 using 600 Hz and 0.033 μf, we get R_1 = 50.5 kΩ. We can use R_{1B} = 47 kΩ and R_{1A} = 10 kΩ. For R_2, we get 101 kΩ. Use R_{2B} = 91 kΩ and R_{2A} = 20 kΩ. To determine R_3, use: $1400 \text{ Hz} = 1/R_3C_0$, which gives us R_3 = 21.6 kΩ. Use R_{3B} = 18 kΩ and R_{3A} = 5 kΩ. R_4 must generate a 300 Hz shift in frequency, the same as R_2. Therefore set R_4 equal to R_2.

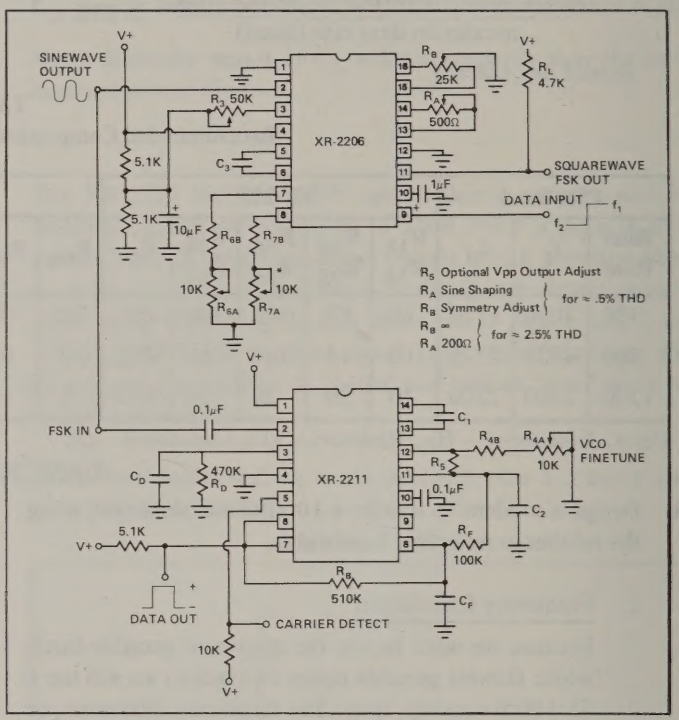


Figure 5. Full Duplex FSK Modem Using XR-2206 and XR-2211. (See Table 2 for Component Values.)

ADJUSTMENT PROCEDURE

The only adjustments that are required with any of the circuits in this application note are those for frequency fine tuning. Although these adjustments are fairly simple and straightforward, there are a couple of recommendations that should be followed.

The XR-2207: Always adjust the lower frequency first with R_{1B} or R_{3B} and a low level on pin 9. Then with a high level on pin 9, adjust the high frequency using R_{2B} or R_{4B}. The second adjustment affects only the high frequency, whereas the first adjustment affects both the low and the high frequencies.

The XR-2206: The upper and lower frequency adjustments are independent so the sequence is not important.

The XR-2211: With the input open-circuited, the loop phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_0 can be monitored:

1. Short pin 2 to pin 10 and measure f_0 at pin 3 with C_D disconnected;
2. Open R_5 and monitor pin 13 or 14 with a high-impedance probe; or
3. Remove the resistor between pins 7 and 8 and find the input frequency at which the FSK output changes state.

Note: Do* NOT *adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

For further information regarding the use of the XR-2207, XR-2206 and XR-2211 refer to the individual product data sheets.

Application Note AN-02

XR-C240 Monolithic PCM Repeater

INTRODUCTION

The XR-C240 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Mega bits per second (Mbps) data rates on T-1 type PCM lines.

The XR-C240 monolithic IC is packaged in hermetic 16-pin DIP package and is designed to operate over a temperature range of –40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-out (ALBO) and equilization, and is insensitive to reflections caused by cable discontinuities.

Compared to conventional repeater designs using discrete components, the XR-C240 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

THE T-1 REPEATER SYSTEM:

The T-1 Repeater Line is designed to provide a transmission capability for 24 two-way voice frequency signals which are transmitted digitally using a Pulse-Code Modulation (PCM) technique. The system operates at a data rate of 1.544 Mbps, with bipolar data pulses. It can operate on either pulp- or polyethylene-insulated paired cable that is either pole mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772kHz is less than 36db. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end crosstalk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The details of the T-1 type PCM systems are well covered in the literature listed in References 1 thru 5.

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator. The XR-C240 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C240 IC's, one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architechture shown in the figure is the same as that utilized in the design of the XR-C240 monolithic IC.

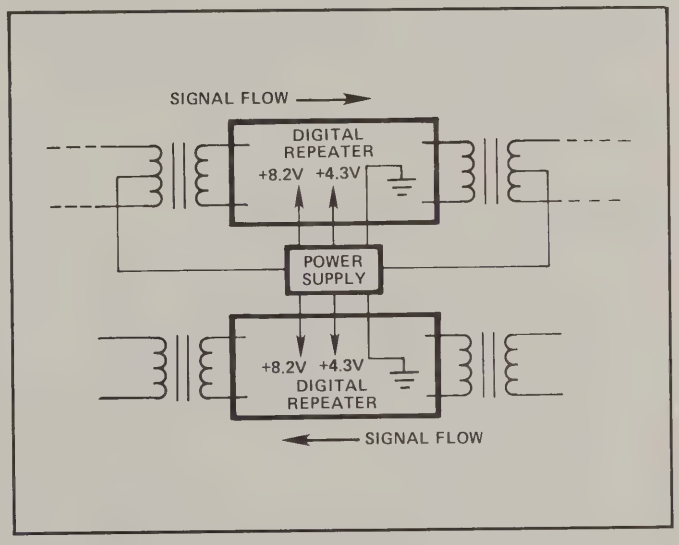


Figure 1. Block Diagram of a Bi-directional Digital Repeater System

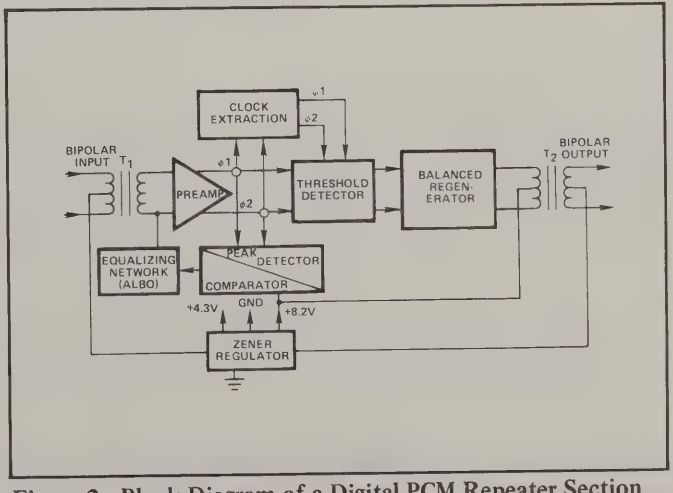


Figure 2. Block Diagram of a Digital PCM Repeater Section

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium, is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization and, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544 MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse is in turn applied to a discrete switch which is used to drive the next section of the paired cable.

REFERENCES ON PCM REPEATERS:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25-97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99-143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1-25.
4. Fultz, K. E. and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405-1452.
5. Tarbox, R. A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 – 46-10.

OPERATION OF THE XR-C240

The XR-C240 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line (DIP) package.

The circuit is designed to operate with two positive supply voltages, V^{++} and V^{+} which are nominally set to be 8.2V and 4.3V, respectively. Figure 4 gives a typical recommended power supply connection for the circuit.

The supply currents I_A and I_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

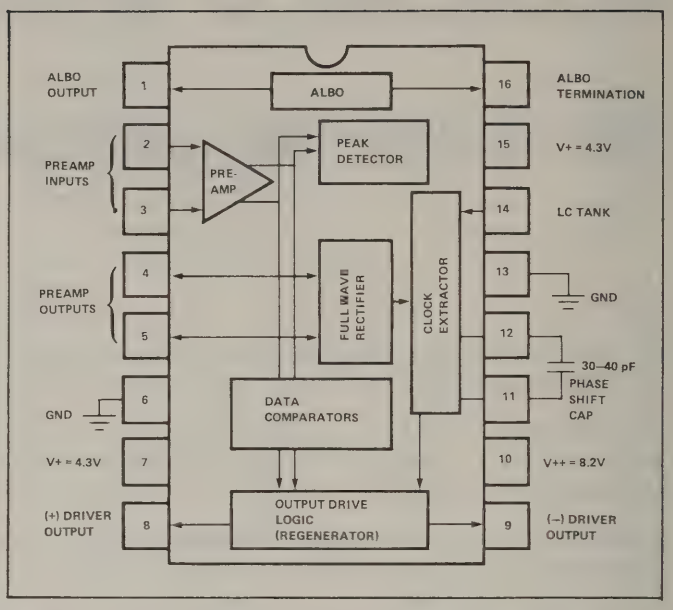


Figure 3. Package Diagram of XR-C240 Monolithic PCM Repeater

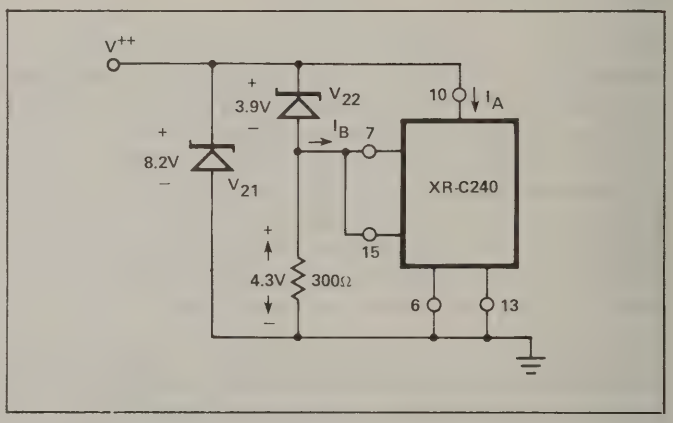


Figure 4. Recommended Supply Voltage Connection for XR-C240 (Note: See Figure 6 for Recommended Bypass Capacitors)

a. Current from 8.2V supply voltage, I_A:

$$1.1\text{mA} \leqslant I_A \leqslant 2.5\text{mA}$$

b. Current from 4.3V supply voltage, I_B:

$$6\text{mA} \leqslant I_B \leqslant 11\text{mA}$$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the system block diagram. Note that all the blocks shown in Figure 6 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 4).

Figure 6 shows a practical circuit connection for the XR-C240 in an actual PCM repeater application for 1.544 Mbps T-1 Repeater application. For simplification purposes, the lightening protection circuitry and the second repeater section are not shown in the figure.

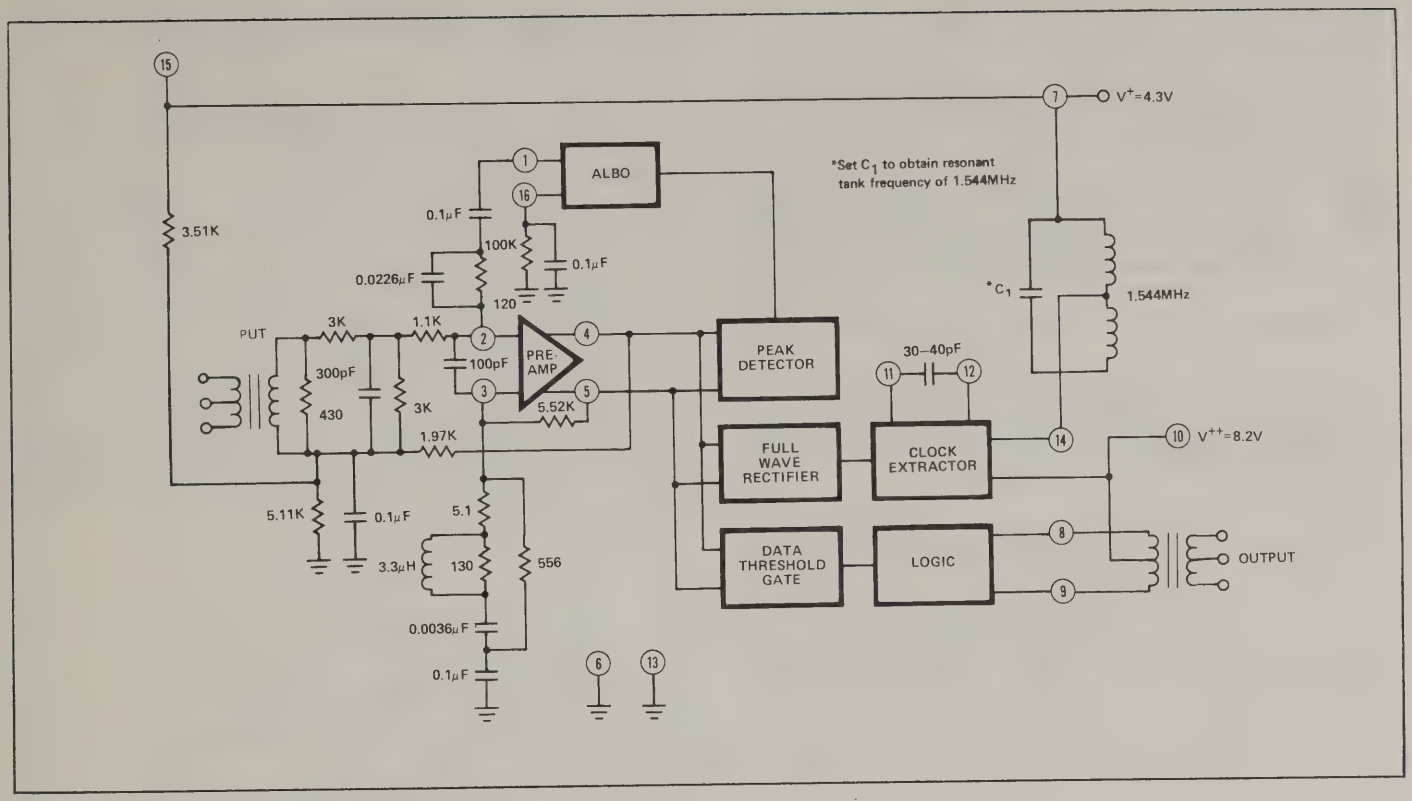


Figure 5. External Components Necessary for Circuit Operation

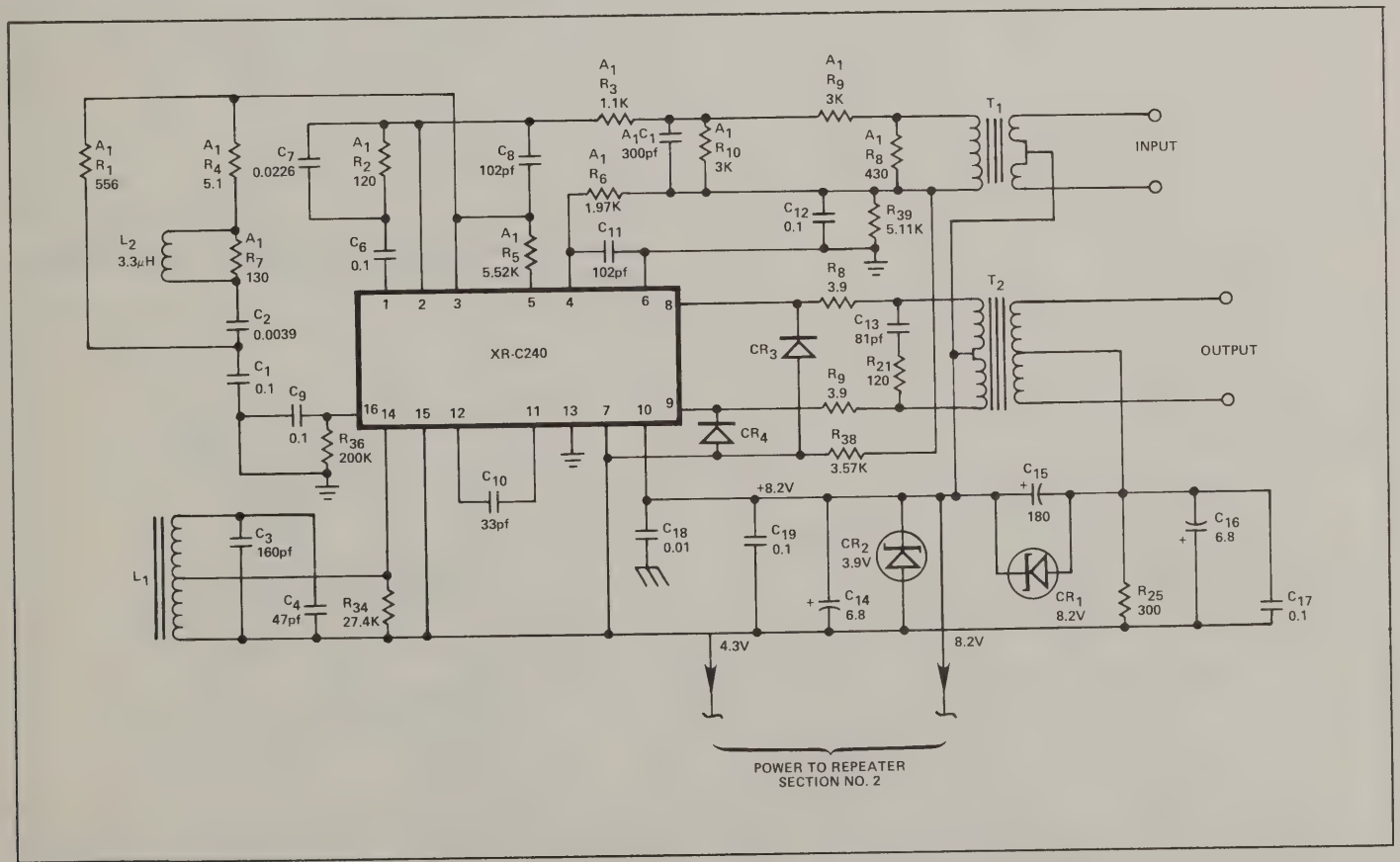


Figure 6. A Typical Circuit Connection for XR-C240 in 1.544 MHz T-1 Repeater System

DESCRIPTION OF CIRCUIT OPERATION:

This section gives a brief description of the internal circuitry contained within the XR-C240 monolithic IC.

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband voltage gain of 52db. The differential outputs of the preamplifier (pins 4 and 5) are internally connected to the peak-detector, full-wave rectifier and the threshold detector sections of the XR-C240 as shown in Figure 8.

The peak-detector output (terminal B of Figure 8) is internally connected to the Automatic Line Build-out (ALBO) section of the circuit and controls the DC bias current through the ALBO diodes Q_{19} through Q_{20}, as shown in Figure 9.

The full-wave rectifier output (output D of Figure 8) is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (pin 14) of the injection locked oscillator. The threshold-detector outputs (G+ and G– of Figure 8) provide the differential logic drive to the data latches of the logic section of XR-C240.

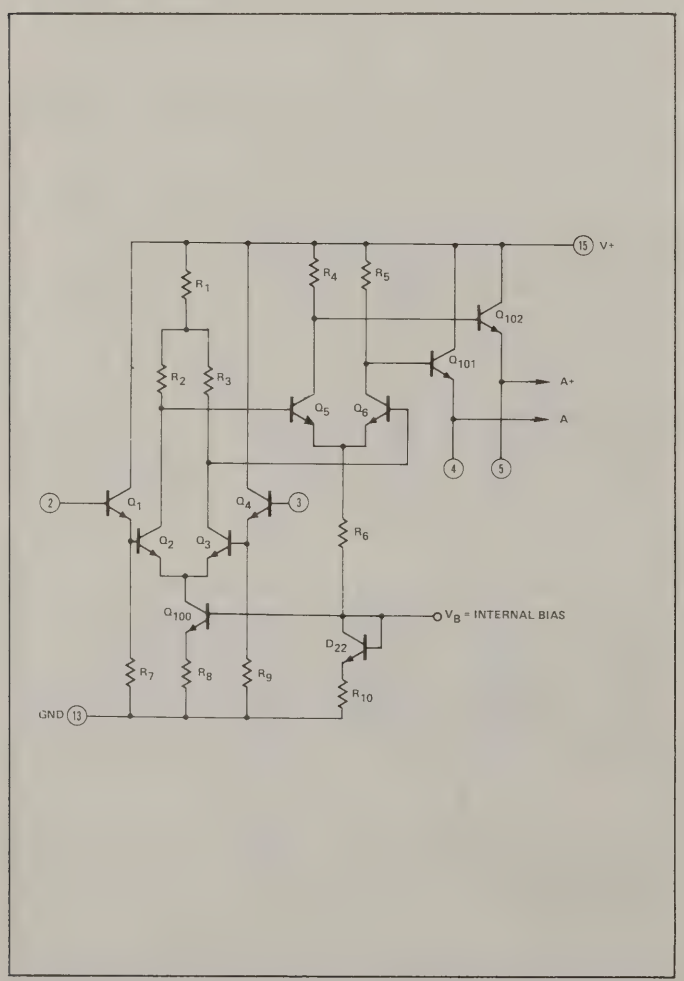


Figure 7. Circuit Diagram of Preamplifier Section

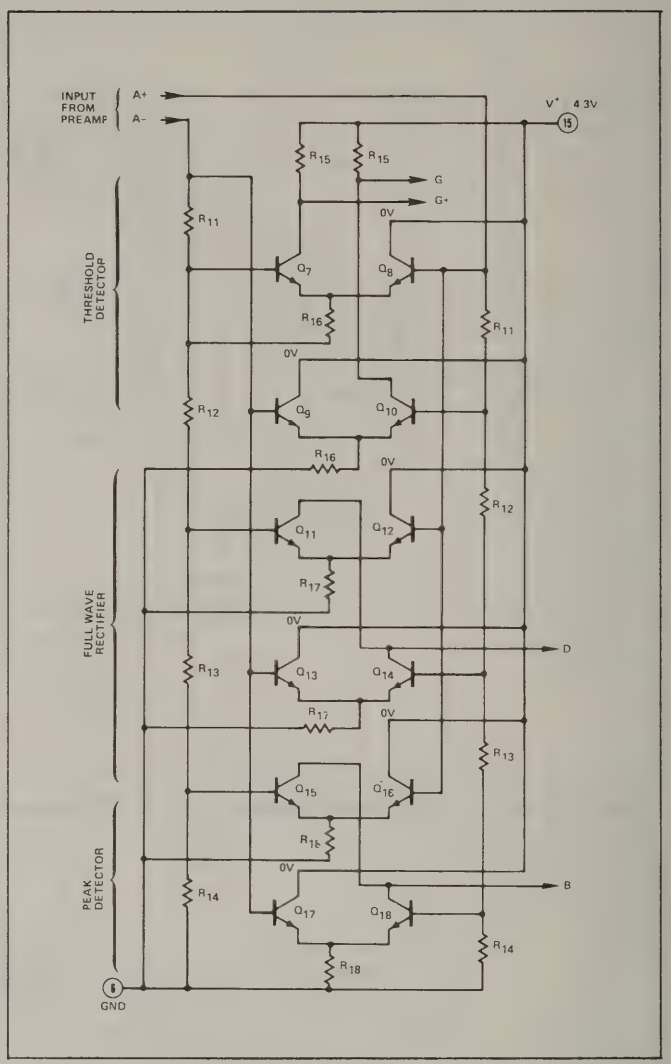


Figure 8. Circuit Diagram of Threshold-Detector, Full-Wave Rectifier and Peak-Detector Sections

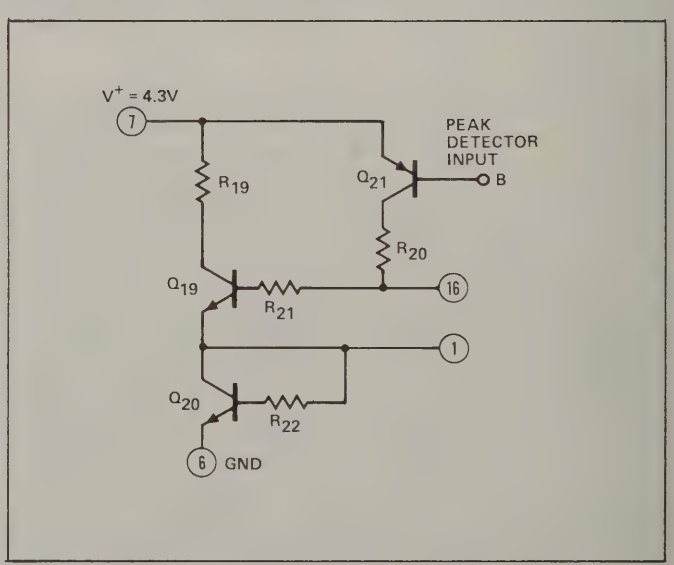


Figure 9. Automatic Line Build-Out (ALBO) Section

The clock-extractor section of XR-C240 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{23}, through terminal D which is internally connected to the output of the threshold comparator. This signal in turn controls the current in the resonant L-C tank circuit connected to pin 14. The sinusoidal waveform across the tank is then amplified and squared through the cascaded differential gain stages made up of Q_{31}, Q_{32} and Q_{35}, Q_{36}. The output swing of the second gain stage is "integrated" by the phase-shift capacitor, C_1, externally connected to pins 11 and 12. (See timing diagrams of Figure 13.) The nominal value of this capacitor is in the 30 to 40pf range. The triangular waveform across pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the "strobe" signal, C_p, and the clock pulse C_ϕ, which is applied to the data latches of the logic section.

The strobe and clock pulses out of the clock-regenerator section are applied to the output data latches shown in Figure 11. The two parallel output R-S flip-flops are driven by the differential inputs (G+ and G–) from the data comparator of Figure 8. The two sets of differential data signals, F_1, $\overline{F}_1$ and F_2, $\overline{F}_2$ are then applied to the output driver amplifier shown in Figure 12. The high-current outputs of the driver stage (pins 8 and 9) are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage spread, i.e.:

$$\text{Peak Output Swing} = (V^{++}) - (V^{+}) - (V_{BE}) \simeq 3.2V$$

The output stage is designed to work into a nominal load impedance of 100 ohms, and can handle peak load currents of 30mA.

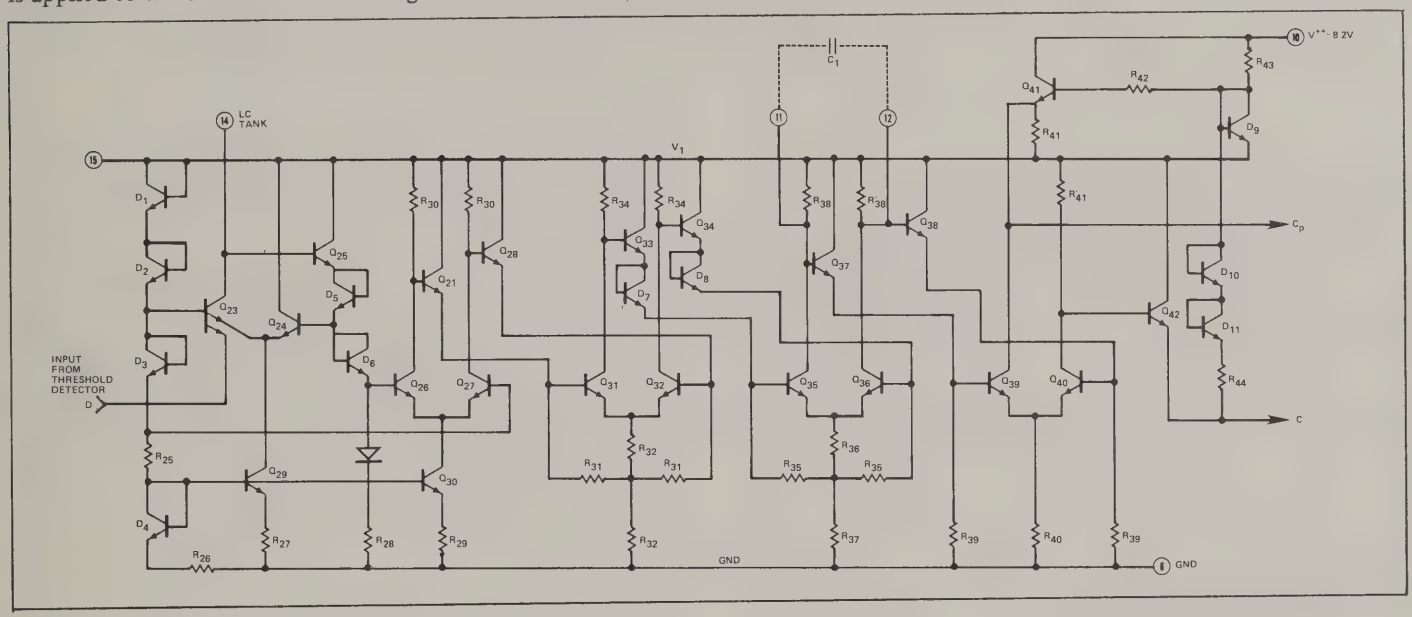


Figure 10. Circuit Diagram of Clock Extractor Section

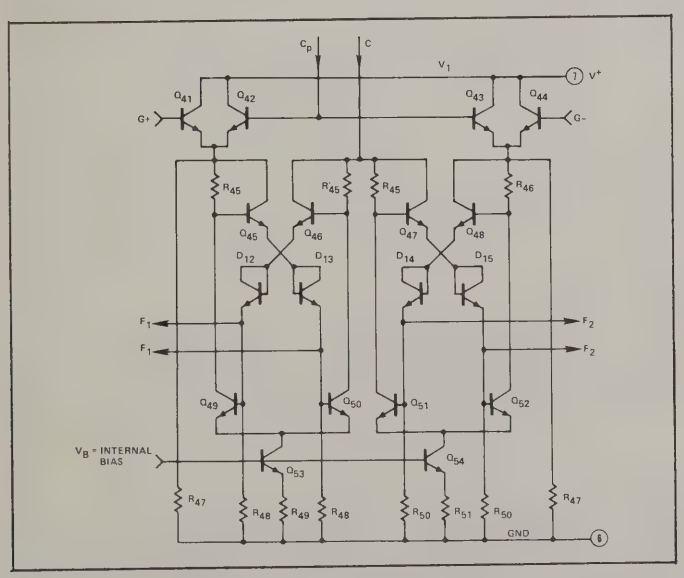


Figure 11. Data Output Latches (Logic Section)

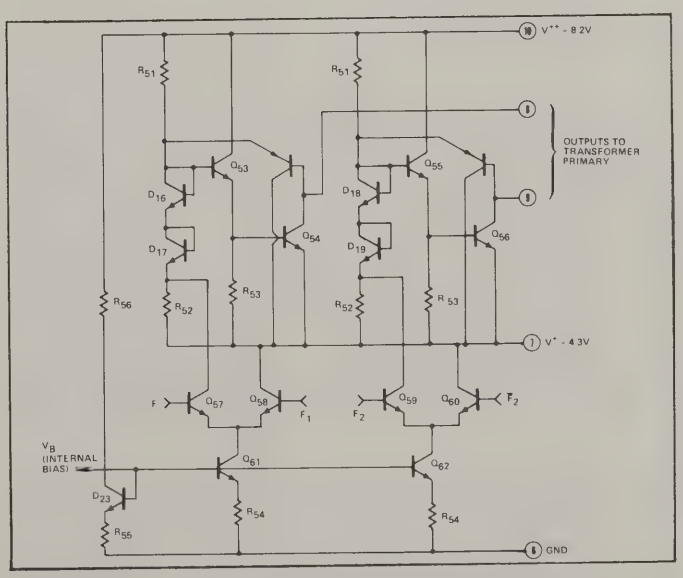


Figure 12. Output Driver Section

Figure 13 shows the typical timing sequence of the circuit waveforms. For illustration purposes, a "one-zero-one" input data pattern is assumed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Power Dissipation	750mW
Derate above +25°C	6mW/°C
Storage Temperature Range	–65°C to +150°C

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-C240	Ceramic	–40°C to +85°C

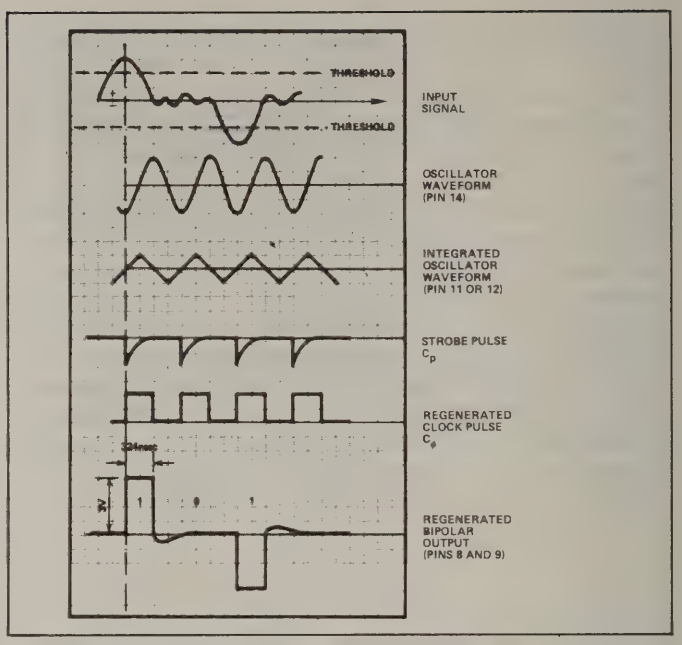


Figure 13. Typical Timing Waveforms for a 1 – 0 – 1 Input Data Pattern

ELECTRICAL CHARACTERISTICS

(Measured at 25°C with V^{++}=8.2V, V^{+}=4.3V, unless specified otherwise.)

CHARACTERISTICS	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
Supply Voltage:				
V^{++}	7.79	8.61	V	Measured at Pin 10
V^{+}	4.085	4.515	V	Measured at Pins 7 and 15
Supply Current:				See Figure 4
I_A	1.1	2.5	mA	Supply = 8.2V
I_B	6	11	mA	Supply = 4.3V
Total Current	7.1	13.5	mA	
Preamplifier				
Input Offset Voltage, V_{OS}		15	mV	
Open Loop Differential Gain, A_O	50	54	db	
Input Bias Current, I_B		4	μA	
Input Offset Current, I_{OS}		2	μA	
Input Impedance, R_{in}	50		kΩ	
Comparator Thresholds				See Figure 8 Measured Differentially Across Pins 4 and 5
Peak Detector (ALBO) Threshold	±1.3	±1.6	V	
Full-Wave Rectifier Threshold	±0.9	±1.15	V	
Data Threshold	±0.28	±0.48	V	
Clock Extractor Section				See Figure 10
Tank Drive Impedance	50		kΩ	At Pin 14
Tank Drive Current				
"Zero" Signal Current	12	24	μA	
"One" Signal Current	80	220	μA	
Recommended Tank Q	100			
Phase Shifter Offset Voltage	–18	+18	mV	Voltage applied to Pins 7 and 14 to reduce differential voltage across Pins 11 and 12 to zero.
Output Drive Section				See Figure 12 Voltage levels referenced to Pin 7
Output Voltage Swing	3.0		V	R_L = 100Ω
Low Output Voltage	0.65	0.95	V	Referenced to Pin 7, I_L = 30mA
Output Leakage Current		50	μA	
Output Pulse				See Figure 13
Maximum Pulse Width Error		±30	nsec	
Rise and Fall Times		80	nsec	

Application Note AN-03

Active Filter Design with IC Op-Amps

INTRODUCTION

This application note is intended to familiarize the filter designer with the fundamentals of active filter design, using monolithic IC op amps. It presents a table of transfer functions and network equations for high-pass, low-pass, band-pass and band-reject filters. Several design examples are given to illustrate the respective merits and limitations of various filter configurations. Particular emphasis is given to applications of programmable quad operational amplifiers, such as the XR-4202, as an active filter element in FSK Modems.

FUNDAMENTALS OF ACTIVE FILTERS

The availability of low cost dual or quad operational amplifier IC's have made the operational amplifier based active filter techniques cost effective over conventional passive filters. The recent availibility of programmable quad operational amplifiers such as the XR-4202 or the XR-346 have provided the active filter designer with the flexibility to externally program gain-bandwidth product, supply current, input bias current, input offset current, input noise and the slew rate. The user, therefore, can trade off bandwidth for supply current or optimize the noise figure. Likewise, other amplifier characteristics can be programmed for a specific need.

Since the operational amplifier plays such a key role in the active filter, its characteristics are of prime importance. By using operational amplifiers as the basic gain stage of the active filter, problems previously encountered due to low input impedance, high output impedance and low gain are virtually eliminated. Operational amplifiers provide the required response for various filter types. Some of the more popular filters are multiple feedback, state variable, bi-quad and Sallen Key which can be used to obtain high pass, band pass and low pass filter functions (and which are capable of giving the designer all of the standard filter responses, i.e., Butterworth, Chebychev, Bessel, etc.)

Table 1 is intended to give the designer a brief review of the basic transfer functions, and network defining equations. It is noted that a family of curves exists for all cases except first order low pass and high pass. This is due to the presence of α, the damping coefficient.

Once the transfer function has been determined, the next step in filter design is to decide upon the desired response. As previously mentioned the damping of the filter determines it's characteristics near cut off. There are three basic types of responses which are depicted in Table 2 along with their characteristics. In the case of the Butterworth and Bessel, the response has been fixed. However, for the Chebychev the α is chosen for the particular response desired. This is done by using a nomograph such as the one shown in Figure 1. To use a nomograph the information required is: A_{max} (maximum ripple in the passband), A_{min} (minimum attenuation in the stop band), and Ω_s (ratio of the A_{min} bandwidth to the A_{max} bandwidth). These terms are illustrated in Figure 2. Once these terms are known the nomograph is used by locating A_{max} and drawing a straight line through A_{min} to the left hand side of the graph. From this point a horizontal line is drawn to the intersection of Ω_s. The minimum order of the transfer function will be the number of the curve passing above this point. Once this is done the α and ωo for each stage is found by consulting the Chebychev network parameter tables for the desired passband ripple, and the number of poles. Such tables can be found in standard filter handbooks.

FILTER REALIZATIONS

There are numerous ways of realizing the transfer functions discussed. Each of these methods have their own relative merits. The configuration selected depends primarily on the specific application and the desired sensitivity parameters. Sensitivity parameters are a means of relating the resultant change in the transfer function due to an element change. Although these parameters are only directly applicable to an infinitesimal change they are easily used to evaluate performance for 1% changes, and many times are used for element changes up to 10%. Examples will be given later in this section that will help clarify this parameter.

The filter realizations presented here are to be used as a basic guide to help the designer to become more adept at designing filters. State-variable and multiple-feedback filters will be discussed and the relative merits of each will be given. It will also be shown that many of the commonly used filters are actually specific cases for the filters mentioned.

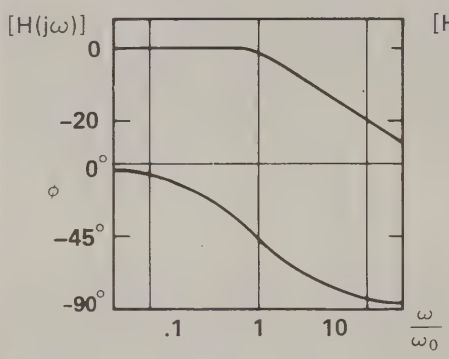
TABLE 1

Low Pass

$$H(s) = \frac{H o \omega o}{s + \omega o}$$

$$[H(j\omega)] = \left[\frac{Ho^2 \omega o}{\omega^2 + \omega o^2}\right]^{1/2}$$

$$\phi = \mathrm{Tan}^{-1} \frac{\omega}{\omega o}$$

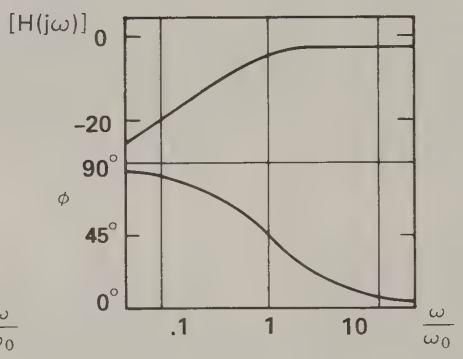


High Pass

$$H(s) = \frac{H o s}{s + \omega o}$$

$$[H(j\omega)] = \left[\frac{Ho^2 \omega o^2}{\omega^2 + \omega o^2}\right]^{1/2}$$

$$\phi = \frac{\pi}{2} - \mathrm{Tan}^{-1} \frac{\omega}{\omega o}$$

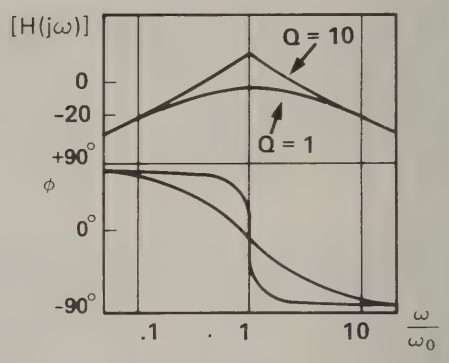


Band Pass

$$H(s) = \frac{Ho\, \alpha\, \omega os}{s^2 + \alpha\omega os + \omega o^2}$$

$$[H(j\omega)] = \left[\frac{Ho^2 \alpha^2 \omega o^2 \omega^2}{\omega^4 + \omega^2 \omega o^2 (\alpha^2 - 2) + \omega o^4}\right]^{1/2}$$

$$\phi = \frac{\pi}{2} - \mathrm{Tan}^{-1}\left(\frac{2Q\omega}{\omega o} + \sqrt{4Q^2 - 1}\right) - \mathrm{Tan}^{-1}\left(\frac{2Q\omega}{\omega o} - \sqrt{4Q^2 - 1}\right)$$

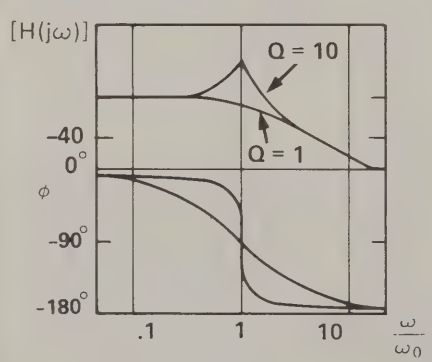


Low Pass Second Order

$$H(s) = \frac{Ho\omega o^2}{s^2 + \alpha\omega os + \omega o^2}$$

$$[H(j\omega)] = \left[\frac{Ha^2 \omega o^4}{\omega^4 + \omega^2 \omega o^2 (\alpha^2 - 2) + \omega oA}\right]^{1/2}$$

$$\phi = -\mathrm{Tan}^{-1}\left[\frac{1}{\alpha}\ 2\frac{\omega}{\omega o} + \sqrt{4 - \alpha^2}\right] - \mathrm{Tan}^{-1}\left[\frac{1}{2}\ \frac{2\omega}{\omega o} - \sqrt{4 - \alpha^2}\right]$$

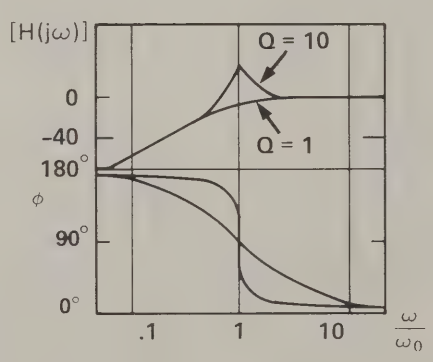


High Pass Second Order

$$H(s) = \frac{Ho s^2}{s^2 + \alpha\omega os + \omega o^2}$$

$$[H(j\omega)] = \left[\frac{Ho^2 \omega^4}{\omega^4 + \omega^2 \omega o2(\alpha^2 - 2) + \omega o^4}\right]^{1/2}$$

$$\phi = \pi - \mathrm{Tan}^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right)\right] - \mathrm{Tan}^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} - \sqrt{4 - \alpha^2}\right)\right]$$

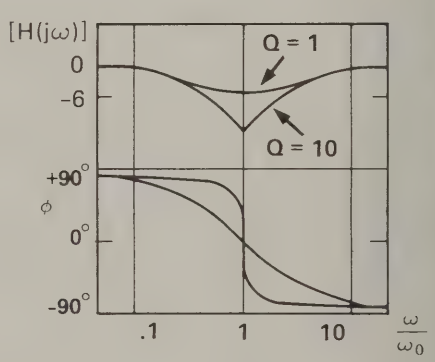


Band Reject

$$H(s) = \frac{(s^2 + \omega o^2) Ho}{s^2 + \alpha\omega os + \omega o^2}$$

$$[H(j\omega)] = \left[\frac{Ho^2 \omega^4 + \omega o^4}{\omega^4 + \omega^2 \omega o(\alpha^2 - 2) + \omega o^4}\right]^{1/2}$$

$$\phi = \frac{\pi}{2} - \mathrm{Tan}^{-1}\left(\frac{2Q\omega}{\omega o} + \sqrt{4Q^2 - 1}\right) - \mathrm{Tan}^{-1}\left(\frac{2Q\omega}{\omega o} - \sqrt{4Q^2 - 1}\right)$$



Definition of Terms

ωo = Cut off frequency $2\pi f_0$

α = Loop damping

$s = \sigma + j\omega$ complex frequency

ω_C = Center frequency

ω_1 = Lower cut off frequency

ω_2 = Upper cut off frequency

$Q = 1/\alpha = \dfrac{\omega c}{\omega_2 - \omega_1}$

ϕ = Phase

$[H(j\omega)]$ = Magnitude response

$H(s)$ = Transfer function

TABLE 2

Filter Type	α	Basic Features	Amp. Response
Bessel	$\sqrt{3}$	Best time delay Smoothest phase response	
Butterworth	$\sqrt{2}$	Maximally flat amplitude response	
Chebychev	Can Vary	Passband ripple Fast cutoff slope	

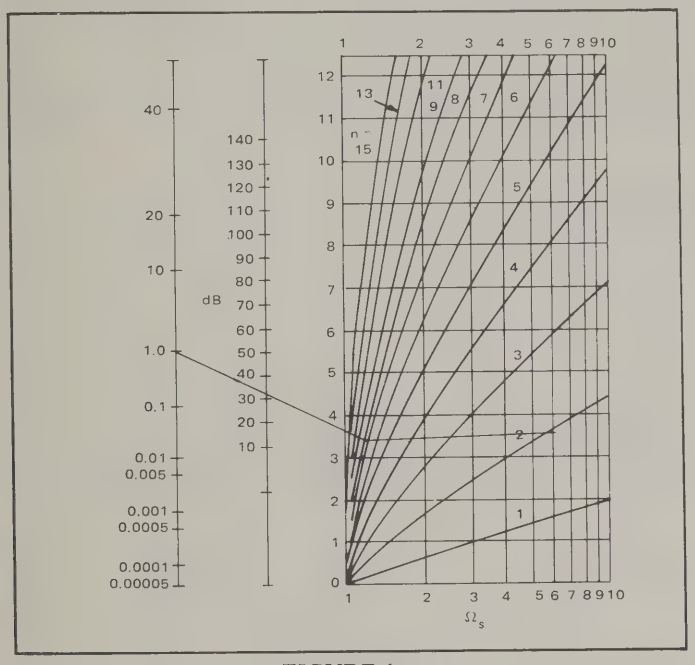


FIGURE 1

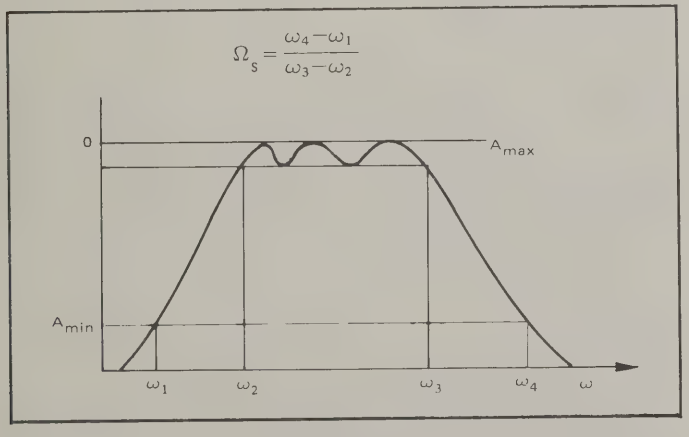


FIGURE 2

Figure 3 illustrates a typical multiple-feedback connection with the non-inverting input grounded. To minimize offset this point should be returned to ground via a resistor whose value is equal to the impedance at the inverting input. The transfer function for this circuit is given by E-1. Each element represents a single resistor or capacitor. To realize the transfer function each admittance parameter is replaced by 1/R for a resistor and sC for a capacitor. An example will help to clarify this point. If the desired response is a high pass, the

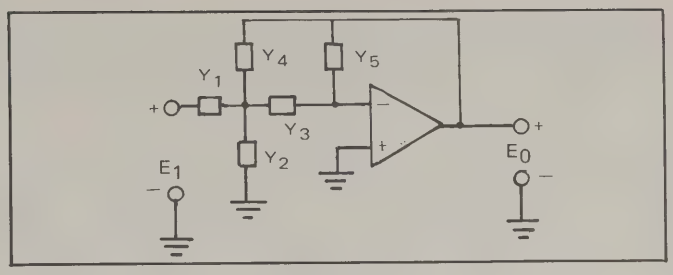


FIGURE 3

E–1
$$\frac{E_0}{E_1}(s) = \frac{-Y_1 Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3 Y_4}$$

form of the characteristic equation is given in Table 1. To transform E–1 into the high-pass characteristic, then Y_1, Y_3, and Y_4 become capacitors and Y_2 and Y_5 resistors. (It should be obvious that a low-pass function could have been fabricated by letting Y_2 and Y_5 be capacitors, and similarly a bandpass function could have been realized by making Y_3 and Y_4 capacitors.) The terms of the network function of the high-pass filter shown in Figure 4 are given in Table 3 along with their sensitivity parameters. The transfer function for Figure 4 is given by E–2.

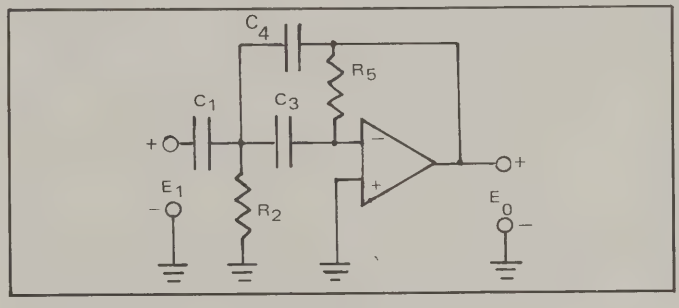


FIGURE 4

E–2
$$\frac{E_0}{E_1}(s) = \frac{-(C_1/C_4)s^2}{s^2 + s(1/R_5)(C_1/C_3C_4 + 1/C_4 + 1/C_3) + 1/R_2R_5C_3C_4}$$

As can be seen from the sensitivity parameters, there is a high degree of circuit sensitivity due to the component tolerances. Due to the interaction of components the tuning of this circuit may be rather involved. However, with tight component tolerances, these circuits give the designer very predictable results. Due to the high input impedance and low output impedance, several of these stages may easily be cascaded to achieve a higher order function. What is desired is to have a lower sensitivity to component tolerances. The most commonly used filter for this purpose is the state-variable.

The state-variable synthesis approach is used in most present day Universal Active Filters (U.A.F.). With this method the actual n^{th} order polynomial of the transfer function is simulated as it would be with an analog computer. When using the state-variable approach all three outputs (high-pass, low-pass and band-pass) are all available simultaneously. The sensitivities with respect to component tolerances are typically less than or equal to one, and the sensitivity of Q

TABLE 3

Parameter	Defining Equation	Sensitivity
H_0	$= \frac{C_1}{C_4}$	$S_{C_1}^{H_0} = -S_{C_4}^{H_0} = 1$
α	$= \sqrt{\frac{R_2}{R_5}} \left(\frac{C_1}{\sqrt{C_3 C_4}} + \sqrt{\frac{C_3}{C_4}} + \sqrt{\frac{C_4}{C_3}} \right)$	$S_{C_3}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha \omega_0 R_5 C_3} \left(\frac{C_1}{C_3} + 1 \right)$ $S_{C_4}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha \omega_0 R_5 C_4} \left(\frac{C_1}{C_3} + 1 \right)$ $S_{C_1}^{\alpha} = \frac{1}{\alpha \omega_0 R_5} \frac{C_1}{C_3 C_4}$ $S_{R_2}^{\alpha} = -S_{R_5}^{\alpha} = \frac{1}{2}$
ω_0	$= \left(\frac{1}{R_2 R_5 C_3 C_4} \right)^{1/2}$	$S_{R_2}^{\omega_0} = S_{R_5}^{\omega_0} = S_{C_3}^{\omega_0} = S_{C_4}^{\omega_0} = -\frac{1}{2}$

Note: The sensitivity of H_0 with This implies that if C_1 changes by 1% H_0 will also change by 1%. The defining equation for a sensitivity parameter is

$$S_X^Y = \frac{x dY}{Y dx}$$

with respect to amplifier gain is nearly zero, if the amplifier gain is high. Because of the high amplifier gain requirement these filters tend to be limited to audio range. The cost of reducing the circuit element sensitivities is the need to use (n + 2) operational amplifiers to synthesize an n^{th} order transfer function. For this reason, this type of configuration may not be cost effective in the synthesis of low Q high-pass and low-pass filters.

Figure 5 shows a typical state-variable configuration whose characteristic equations are given by E–3, E–4, and E–5. It is noted that these equations all have the same denominators; and the numerator is determined by the point at which the output is taken. This form may also be used to simulate a band-reject function by summing the high-pass and low-pass outputs. The defining equations and sensitivity parameters are given in Table 4. It is noted here that the bi-quad is actually a slight variation of a second order state-variable.

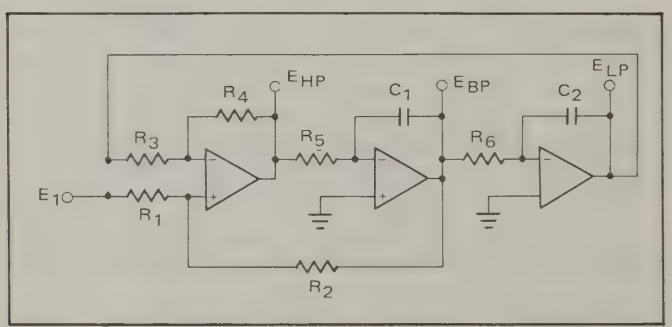


FIGURE 5

E–3
$$\frac{E_{LP}}{E_1} = \frac{\left(\frac{1}{R_5 R_6 C_1 C_2}\right)\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5 C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5 R_6 C_1 C_2}\right)}$$

E–4
$$\frac{E_{HP}}{E_1} = \frac{s^2\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5 C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5 R_6 C_1 C_2}\right)}$$

E–5
$$\frac{E_{BP}}{E_1} = \frac{-s\left(\frac{1}{R_5 C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5 C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5 R_6 C_1 C_2}\right)}$$

MODEM FILTER

A typical application for an active filter is the input stage of a frequency demodulator. Any noise or spurious signals at this point would affect the overall quality of the output. A more specific example can be cited by considering the F.S.K. system shown in Figure 6. (Frequency shift keying is a means of transmitting digital information, primarily through telecommunications links.) This type of system is thoroughly covered in Exar Application Note, AN-01 and will only be briefly discussed here.

In this system, the digital data to be transmitted is used to key the XR-2206. The frequency shift keyed output of the XR-2206 is then sent through the hybrid and out on to the line. (The hybrid is used to obtain isolation between data transmitted and data received, and also may be used to amplify the received signal.) In full duplex operation this system must be able to receive and transmit simultaneously. Due to line losses, the received signal may range from –12 dBm to –48 dBm. The output level of the transmitter is typically –6 dBm (allowing for a 6 dB loss in the hybrid), due to line mismatch, the hybrid may only provide 10 dB of isolation to the filter. (Therefore, the levels at the input of the filter, assuming a gain of 6 dB from the line through the hybrid is –6 and

TABLE 4

Output	Parameters	Defining Equation	Sensitivity
Low Pass E-3	H_0	$\frac{1 + R_3/R_4}{1 + R_1/R_2}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1/(1 + R_2/R_1)$ $S_{R_3}^{H_0} = -S_{R_4}^{H_0} = \frac{1}{H_0}\left(\frac{R_3/R_4}{1 + R_1/R_2}\right)$
	ω_0	$\left[\frac{R_4}{R_3 R_5 R_6 C_1 C_2}\right]^{1/2}$	$S_{R_3}^{\omega_0} = S_{R_5}^{\omega_0} = S_{R_6}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -S_{R_4}^{\omega_0} = -\frac{1}{2}$
	α	$\frac{1 + R_4/R_3}{1 + R_2/R_1}\left(\frac{R_3 R_6 C_2}{R_4 R_5 C_1}\right)^{1/2}$	$S_{R_4}^{\alpha} = -S_{R_3}^{\alpha} = -\frac{1}{2} + \frac{R_4/R_3}{R_5 C_1 \alpha\omega_0 (1 + R_2/R_1)}$ $S_{R_1}^{\alpha} = -S_{R_2}^{\alpha} = \frac{1}{1 + R_1/R_2}$ $S_{R_6}^{\alpha} = S_{C_2}^{\alpha} = -S_{R_5}^{\alpha} = -S_{C_1}^{\alpha} = \frac{1}{2}$
High Pass E-4	H_0	$\frac{1 + R_4/R_3}{1 + R_1/R_2}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1/(1 + R_2/R_1)$ $S_{R_3}^{H_0} = -S_{R_4}^{H_0} = \frac{1}{H_0}\left(\frac{R_4/R_3}{1 + R_1/R_2}\right)$
	ω_0	SAME AS LOW PASS	
	α	$\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right)\left(\frac{R_3 R_6 C_2}{R_4 R_5 C_1}\right)^{1/2}$	$S_{R_4}^{\alpha} = -S_{R_3}^{\alpha} = -\frac{1}{2} + \frac{R_4/R_3}{R_5 C_1 \alpha\omega_0 (1 + R_2/R_1)}$ $S_{R_1}^{\alpha} = -S_{R_2}^{\alpha} = \frac{1}{1 + R_1/R_2}$ $S_{R_6}^{\alpha} = S_{C_2}^{\alpha} = -S_{R_5}^{\alpha} = -S_{C_1}^{\alpha} = 1/2.$
Band Pass E-5	H_0	$\frac{R_2}{R_1}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1$
	ω_0	SAME AS LOW PASS	
	$Q = 1/\alpha$	$\left(\frac{1 + R_2/R_1}{1 + R_4/R_3}\right)\left(\frac{R_4 R_5 C_1}{R_3 R_6 C_2}\right)^{1/2}$	$S_{R_5}^{Q} = S_{C_1}^{Q} = -S_{R_6}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}$ $S_{R_4}^{Q} = S_{R_3}^{Q} = \frac{1}{2} - \frac{R_4/R_3}{R_5 C_1 \alpha\omega_0 (1 + R_2/R_1)}$ $S_{R_2}^{Q} = -S_{R_1}^{Q} = \frac{1}{1 + R_1/R_2}$

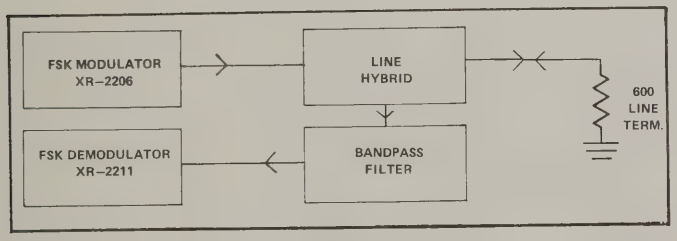


FIGURE 6

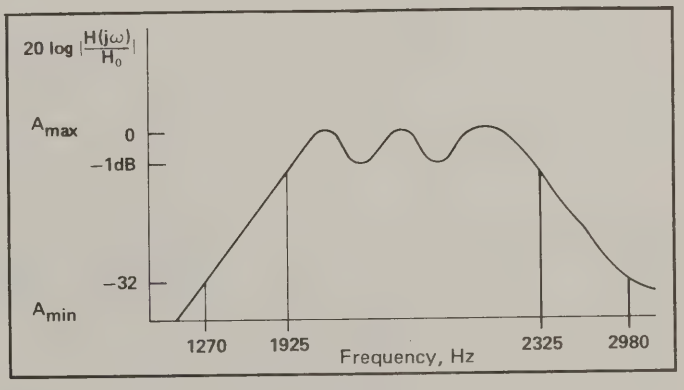


FIGURE 7

−42 dBm for the desired signal and −16 dBm from the local oscillator.) This means that in a worst case situation, the input level of the received signal is −42 dBm with the level of the local oscillator 26 dB above this. For the XR-2211 to operate with a low bit error rate, the input should be 6 dB higher than the interfering signal. This implies that the stopband A_{min} from Figure 2 is 32 dB. The XR-2211 has an internal preamplifier with a dynamic range of greater than 60 dB, and requires a minimum input level of −38 dBm to cause limiting. If we choose a filter to have a passband ripple of 1 dB and an overall gain of 5 dB, the input conditions of the XR-2211 will be satisfied. The filters introduce a phase shift that is only linear for approximately 1/2 to 1/3 of the passband, therefore, a bandwidth of 400 Hz is used for the filter. The general shape of the filter is shown in Figure 7.

Note: The values used in this filter are based on a modem using an XR-2206 as the modulator and XR-2211 as the demodulator. If digital techniques are used, the filter parameters may be different due to the harmonics generated by digital synthesis of a sine wave and higher signal to noise requirements of the demodulator.

To find the minimum number of poles required for this response the nomograph in Figure 1 is used. The point falls between a 2 and 3 pole filter. The values of $\omega_0 + \alpha$ are determined from the tables for a 3rd order chebychev response with 1 dB ripple.

From tables

$\left.\begin{array}{l}\omega_0 = .997098 \\ \alpha = .495609 \\ \omega_0 = .494171\end{array}\right\}$ complex pole
– real pole.

The geometric center is $\omega_0 = \sqrt{\omega_3 \omega_2}$ or $\sqrt{f_3 f_2} = f_0$

The filter $Q_0 = Q_0 = \dfrac{f_0}{f_3 - f_2} = \dfrac{\sqrt{(1925)(2325)}}{2325 - 1925} = 5.28892$

The Q of each section of the filter is determined by Equation 6.

E–6

$$QA = \left(\frac{\left(\frac{\omega_1}{Q_0}\right)^2 + 4 + \sqrt{\left[\left(\frac{\omega_1}{Q_0}\right)^2 + 4\right]^2 - 4\left(\frac{\alpha_1 \omega_1}{Q_0}\right)^2}}{2\left(\frac{\alpha_1 \omega_1}{Q_0}\right)^2} \right)^{1/2}$$

$Q_1 = 21.49 = Q_2$ Section 2 is a reflection of section one about f_0. The center frequencies are found by E–7.

E–7

$$M = \frac{\alpha \omega_1 Q_1}{2Q_0} + \sqrt{\left(\frac{\alpha \omega_1 Q_1}{2Q_0}\right)^2 - 1}$$

Where $M = \dfrac{\omega_1}{\omega_0} = \dfrac{\omega_0}{\omega_2} = \dfrac{f_1}{f_0} = \dfrac{f_0}{f_2}$

$M = 1.0955$
$f_1 = 2317.6$
$f_2 = 1931.1$

for Section 3 the real pole is transformed into a complex pole pair.

$$Q_3 = \frac{2Q_0}{\alpha \omega_B} = 10.7$$

and $f_3 = f_0$.

The 3 filter stages are now defined:

$f_1 = 2317.6$	$Q_1 = 21.49$
$f_2 = 1931.1$	$Q_2 = 21.49$
$f_3 = 2115.56$	$Q_3 = 10.7$

In this example the multiple-feedback approach is used since 3 pole pairs can be generated with 3 op-amps, 6 capacitors and 9 resistors; an equivalent filter could have been designed with the state-variable techniques, but this would have required 9 op-amps to realize. The actual filter is shown in Figure 8. All capacitor values are chosen to be .01 μf, 5% and all resistors are 1%. The values for this filter and a low band filter are shown in Table 5.

TABLE 5

		f_0	ω_0	Q_0	R_1	R_2	R_3	C_1	C_2	H_0
	A	1931.1	12.1335K	21.49	88.6K	192	354K	.01	.01	2
Originate	B	2317.6	14.562K	21.49	74K	160	295K	.01	.01	2
	C	2115.6	13.293K	10.7	40K	355	161K	.01	.01	2
	1									2
Answer	A	1362.26	10.115K	11.827	58.5K	421	234K	.01	.01	2
	B	975.51	6129.3	11.827	96.5K	695	386K	.01	.01	2
	C	1152.78	7.243K	5.832	40.3K	1219.5	161K	.01	.01	2

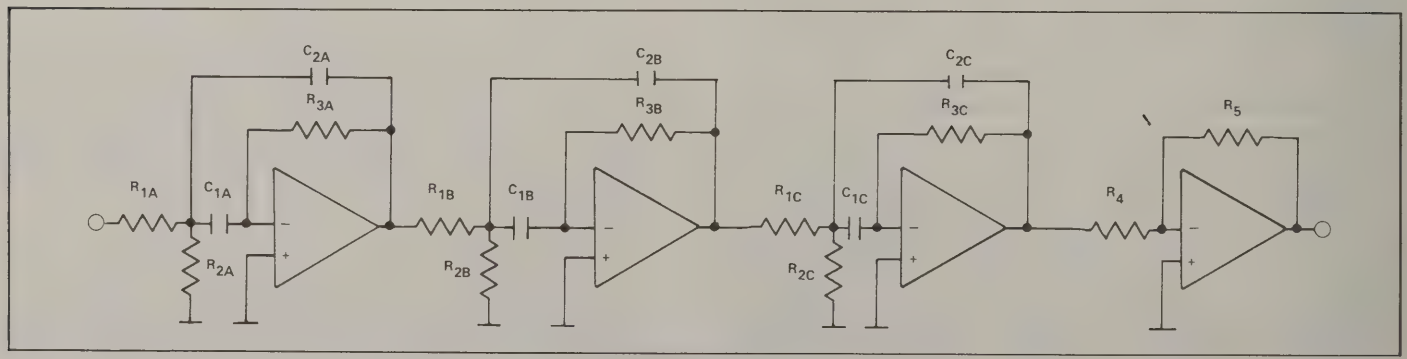


FIGURE 8

Figure 9 shows a circuit schematic for a complete "Originate or Answer" modem. The values for the XR-2206 are given in Table 6. For an originate modem the transmitting frequencies are 1070 Hz and 1270 Hz, the receiving frequencies are 2025 Hz and 2225 Hz, for a space and mark respectively.

The first op amp in Figure 4 is connected as an active hybrid which should supply a minimum of 10 dB isolation from transmit to receive, while adding 10 dB gain from the line to the receiver.

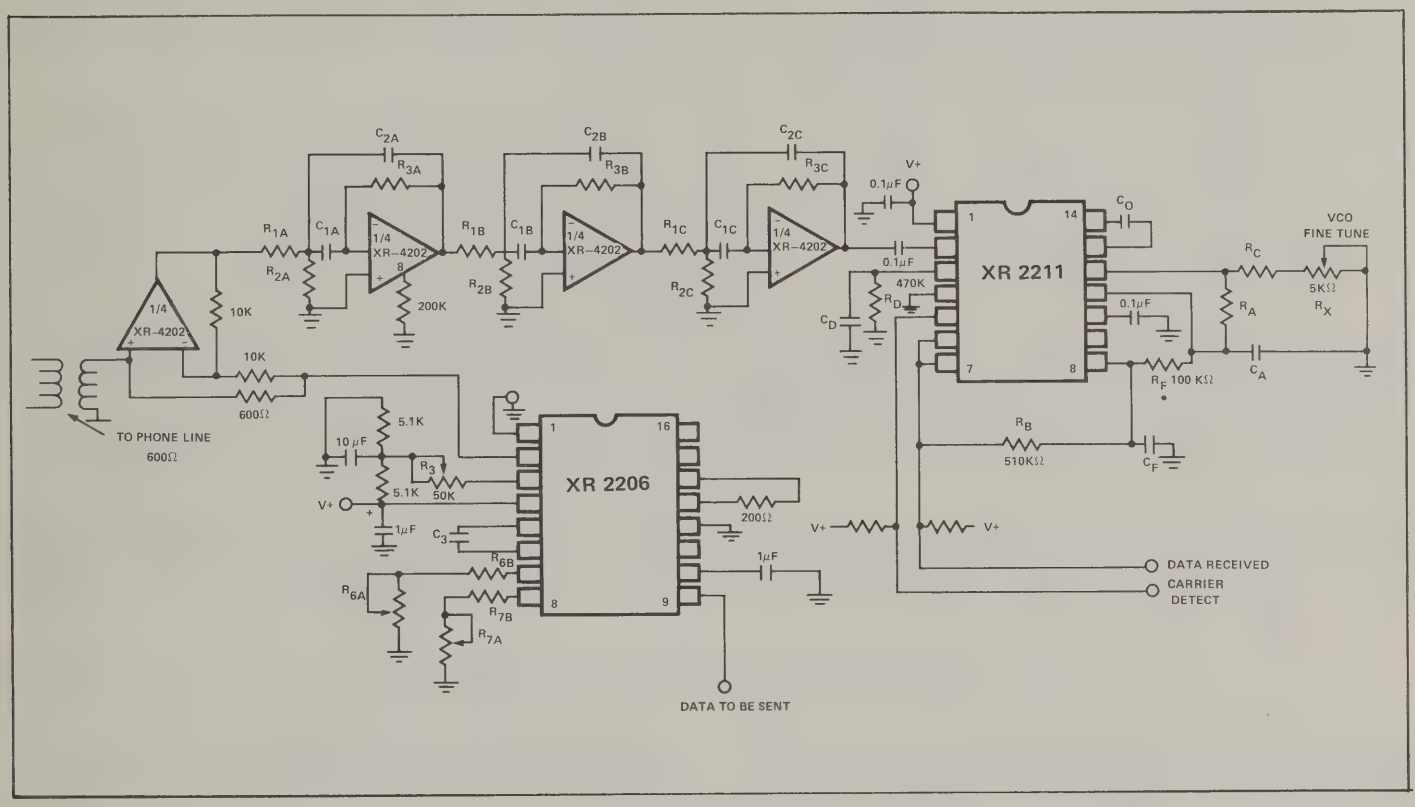


FIGURE 9

TABLE 6
Recommended Component Values for Typical FSK Bands
Units: Frequency – Hz; Resistors – kΩ; Capacitors – μF.

FSK Band			Component Values											
			XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_X	R_C	R_A	C_O	C_A	C_F	C_D
Originate	1070	1270	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
Answer	2025	2225	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05

Application Note AN-04

XR-C277 Low-Voltage PCM Repeater IC

INTRODUCTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Mega bits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltages (6.3 volts and 4.4 volts) with a supply current of less than 13 mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

FUNDAMENTALS OF PCM REPEATERS

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator. The XR-C277 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C277 IC's, one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C277 monolithic IC.

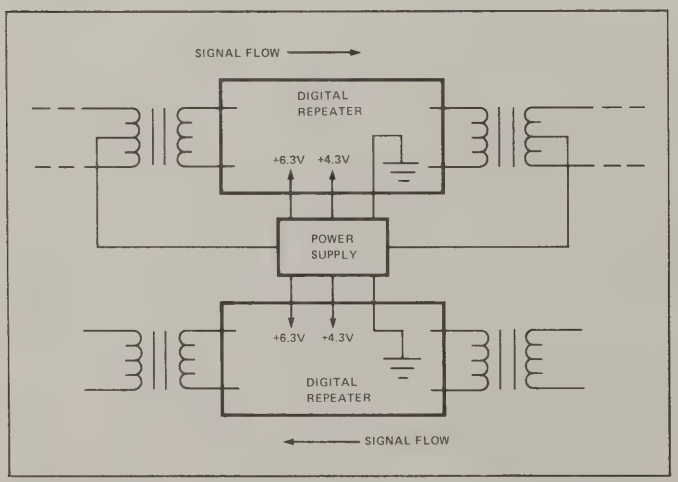


Figure 1. Block Diagram of a Bi-Directional Digital Repeater System

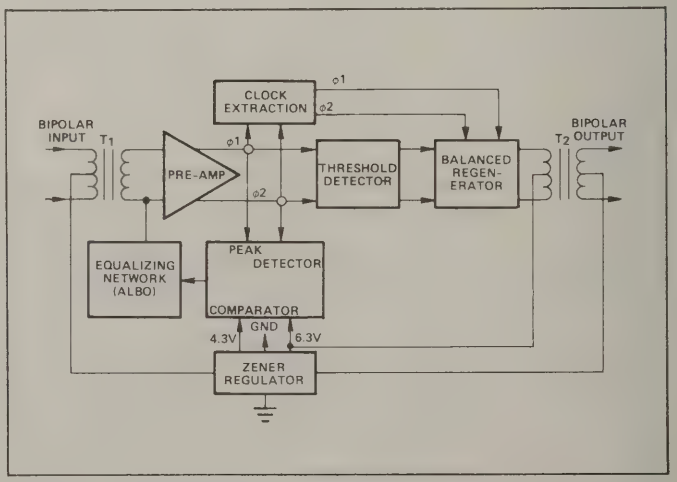


Figure 2. Functional Block Diagram of a Digital PCM Repeater System

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium, is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization and, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544 MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse is in turn applied to a discrete output transformer which is used to drive the next section of the paired cable.

Additional References on PCM Repeaters:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25-97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99-143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1-25.
4. Fultz, K. E. and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405-1452.
5. Tarbox, R.A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 – 46-10.

OPERATION OF THE XR-C277

The XR-C277 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line package.

The circuit is designed to operate with two positive supply voltages, V^{++} and V^{+} which are nominally set to be 6.3V and 4.4V, respectively. Figure 4 gives the recommended power supply connection for the circuit.

The supply currents I_A and I_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 6.3V supply voltage, I_A:

$$2.5\ mA \leqslant I_A \leqslant 4.0\ mA$$

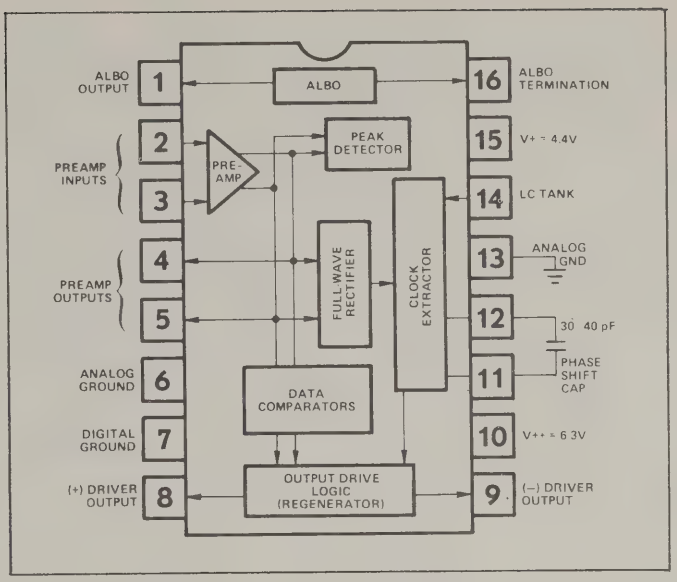


Figure 3. Package Diagram of XR-C277 Monolithic PCM Repeater

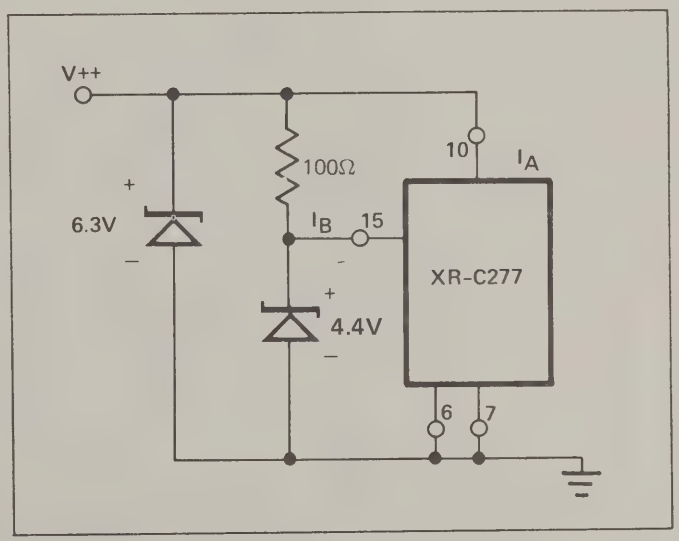


Figure 4. Recommended Supply Voltage Connection for XR-C277 (Note: See Figure 6 for Recommended Bypass Capacitors)

b. Current from 4.3V supply voltage, I_B:

$$7\ mA \leqslant I_B \leqslant 9\ mA$$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the system block diagram. Note that all the blocks shown in Figure 5 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 3).

Figure 6 shows a practical circuit connection for the XR-C277 in an actual PCM repeater application for 1.544 Mbps T-1 Repeater application. For simplification purposes, the lightning protection circuitry and the second repeater section are not shown in the figure.

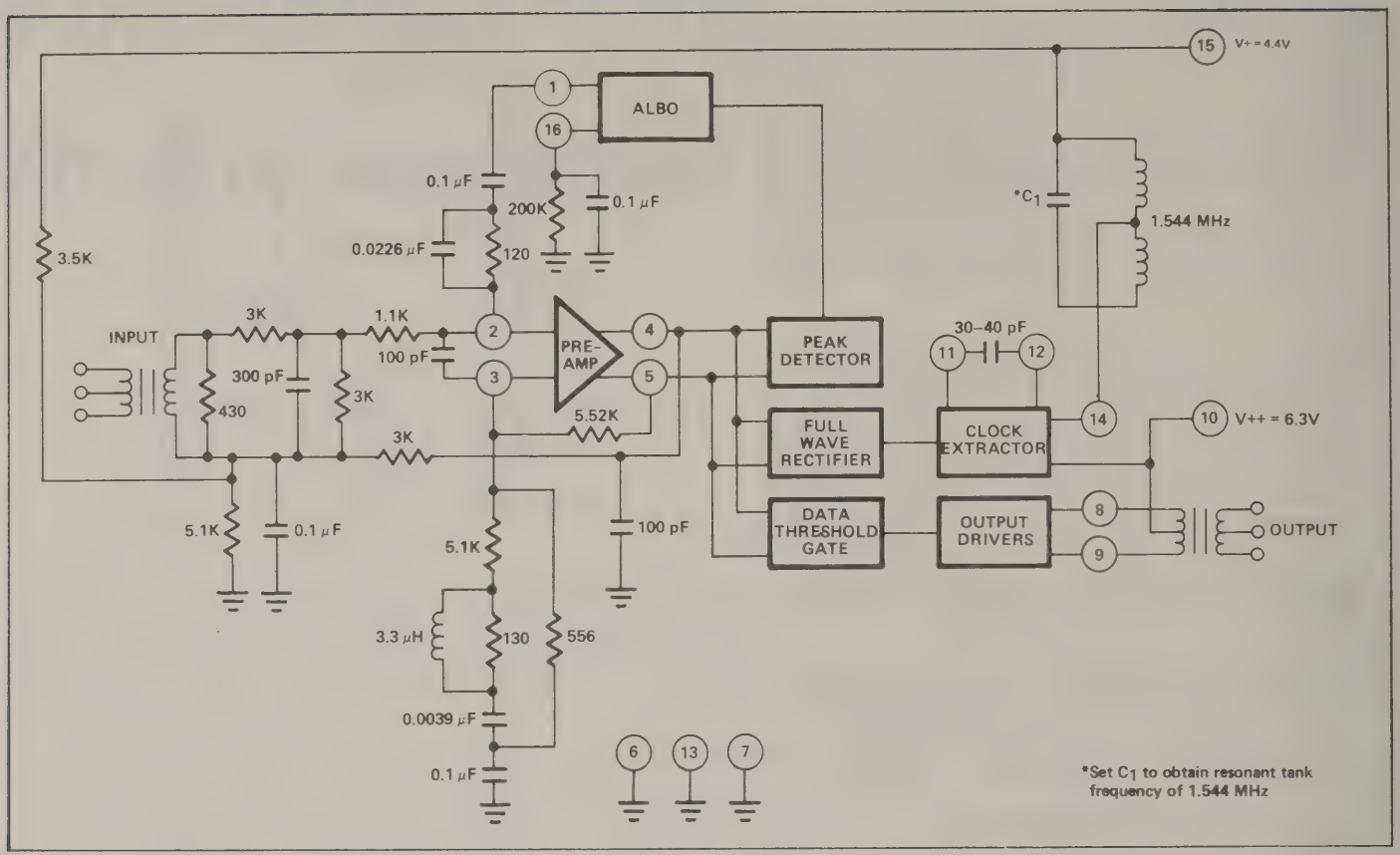


Figure 5. External Components Necessary for Circuit Operation in 1.544 MHz T-1 Repeater

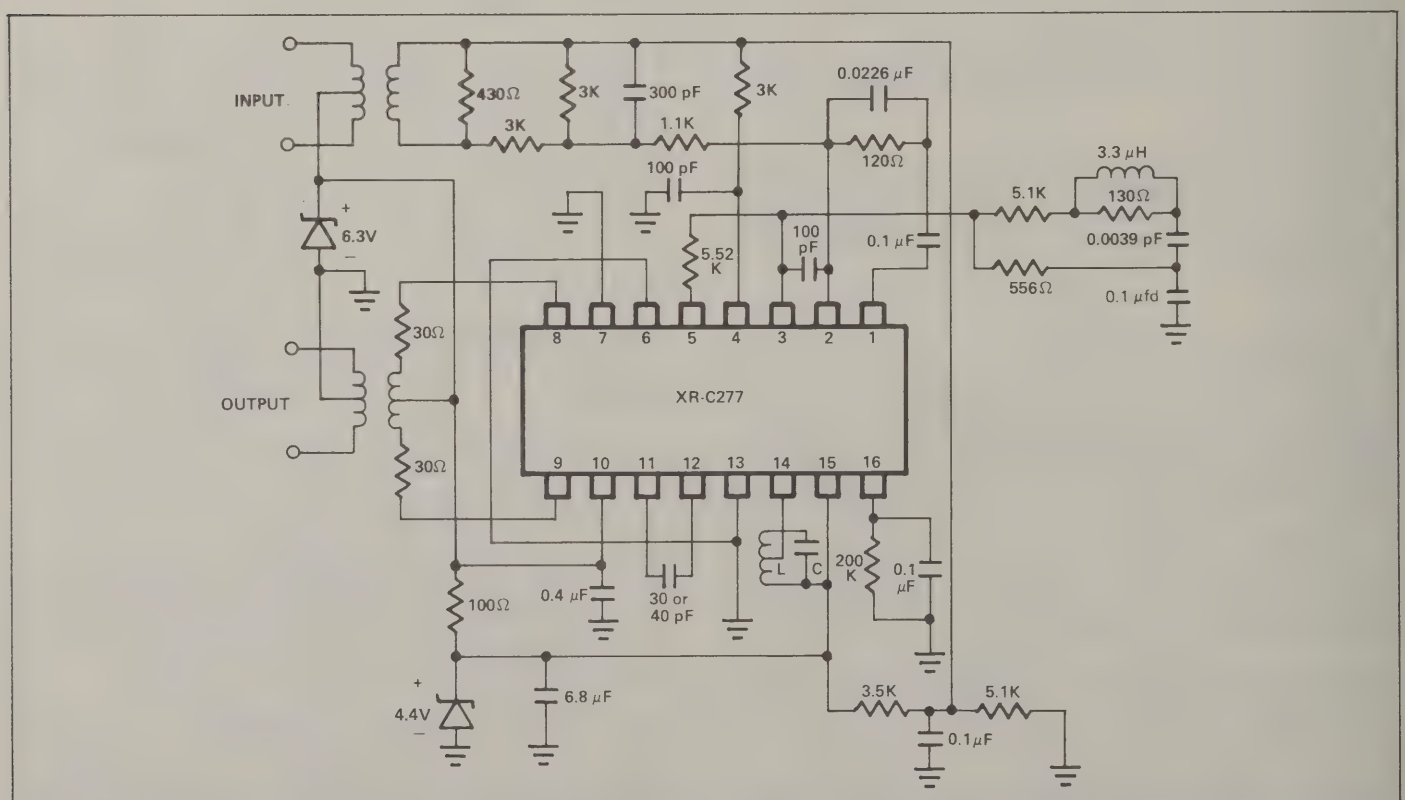


Figure 6. Typical Circuit Connection of XR-C227 in 1.544 MHz T-1 Repeater System. (Note: Set L and C to form a high Q tank resonant at 1.544 MHz. It is recommended that Q < 100, and C ≈ pF for most applications).

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Fig. 7):

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband differential voltage gain of 52 db. The differential outputs of the preamplifier (pins 4 and 5) are internally connected to the peak-detector, full-wave rectifier and the data threshold detector sections of the XR-C277.

Automatic Line Build-Out (ALBO) Section (Fig. 8):

The ALBO function is achieved by controlling the dynamic impedance of ALBO diodes (Q_{21} and Q_{22}). The current whic sets this dynamic impedance is supplied through Q_{21} and is controlled by the peak-detector output level applied to base of Q_{23}.

Data-Threshold Detector; Full-Wave Rectifier and Peak Detector Sections (Figure 9):

The level detector and peak rectifier sections of the XR-C277 are made up of two sets of gain stages which are driven differentially with the (A^+) and (A^-) outputs of the preamplifier section. The outputs of the data threshold comparators, D^+ and D^- activate the data latches shown in Figure 11.

The peak-detector output (terminal B of Figure 9) is internally connected to the Automatic Line Build-Out (ALBO) section of the circuit and controls the DC bias current through the ALBO diodes Q_{21} through Q_{22}, as shown in Figure 8.

The full-wave rectifier output is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (pin 14) of the injection locked oscillator. The detection thresholds of the comparators are set by the resistor chains (R_{45}, R_{47}, R_{51}, R_{55}) and (R_{46}, R_{48}, R_{52}, R_{56}). The resistor ratios are chosen such that the data threshold is 50% of the ALBO threshold; and the clock extractor threshold is 73% of the ALBO threshold.

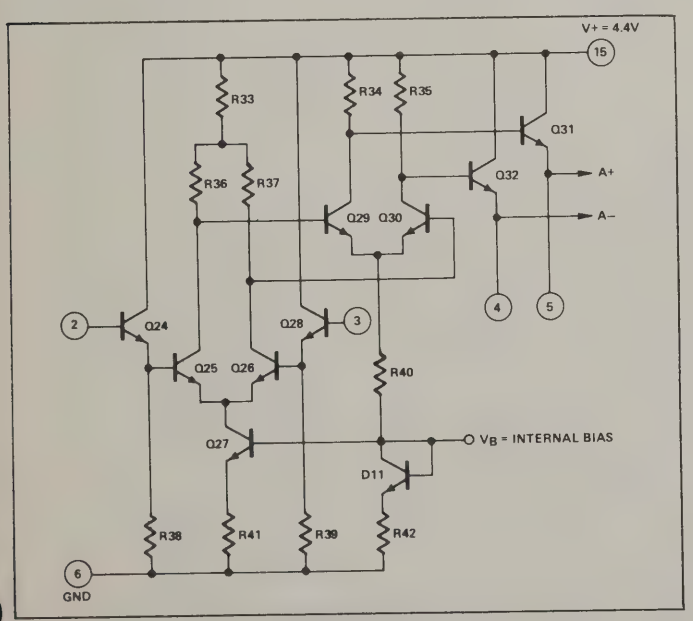


Figure 7. Circuit Diagram of Preamplifier Section

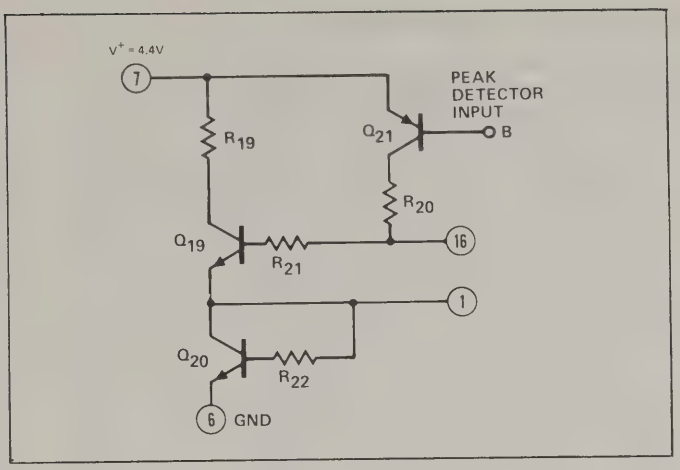


Figure 8. Automatic Line Build-Out (ALBO) Section

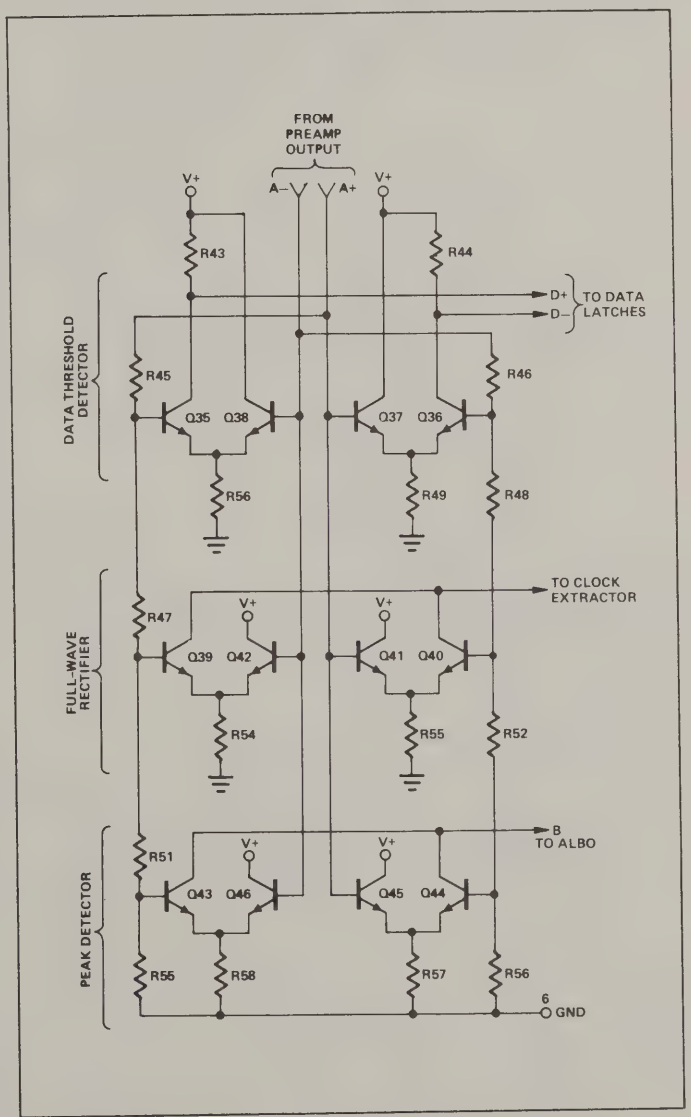


Figure 9. Data-Threshold Detector, Full-Wave Rectifier and the Peak Detector Sections of XR-C277

Clock Extractor Section (Figure 10):

The clock-extractor section of XR-C277 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{1B}, from the output of the full-wave rectifier. This signal in turn controls the current in the resonant L-C tank circuit connected to pin 14. The sinusoidal waveform across the tank is then amplified and squared through two cascaded differential gain stages made up transistors Q_3 through Q_9. The output swing of the second gain stage is "integrated" by the phase-shift capacitor, C_1, externally connected to pins 11 and 12. (See timing diagrams of Figure 13.) The nominal value of this capacitor is in the 30 to 40 pf range. The triangular waveform across pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the "strobe" signal, C_p, and the clock pulse C_ϕ, which are applied to the data latches of the logic section.

Data-Latch and Output Driver Sections (Figures 11 and 12):

The data-latch section consists of two parallel flip-flops, driven by the (D^+) and (D^-) inputs from the data-threshold detector. When the D+ input is at a "low" state, the sampling or strobe pulse, C_p, is steered through Q_{47A} and sets flip-flop 1, on the leading edge of C_p. Conversely, when D^- input is at a "low" state, the sampling pulse is steered through Q_{47B} to set flip-flop 2. Each flip-flop section is then reset at the trailing edge of the clock pulse input, C_ϕ. The flip-flop outputs, (F_1, $\bar{F}_1$) and (F_2, $\bar{F}_2$) are then used to drive the output drivers. This logic arrangement results in an output pulse width which is the same as the extracted clock pulse width (see timing diagram of Figure 13).

The outputs of the two data latches drive the two output driver stages shown in Figure 12. The high-current outputs of the driver stage (pins 8 and 9) are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage at pin 10. The output stages are designed to work into a nominal load impedance of 100 ohms, and can handle peak load currents of 30 mA.

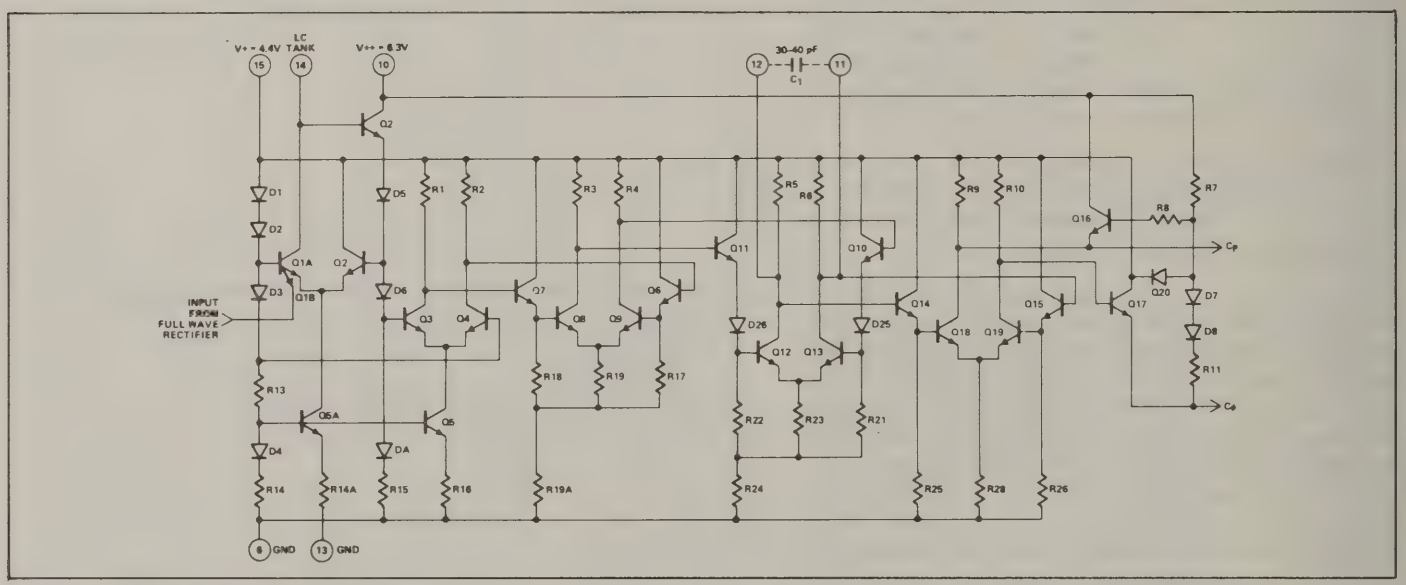


Figure 10. Circuit Diagram of Clock Extractor Section

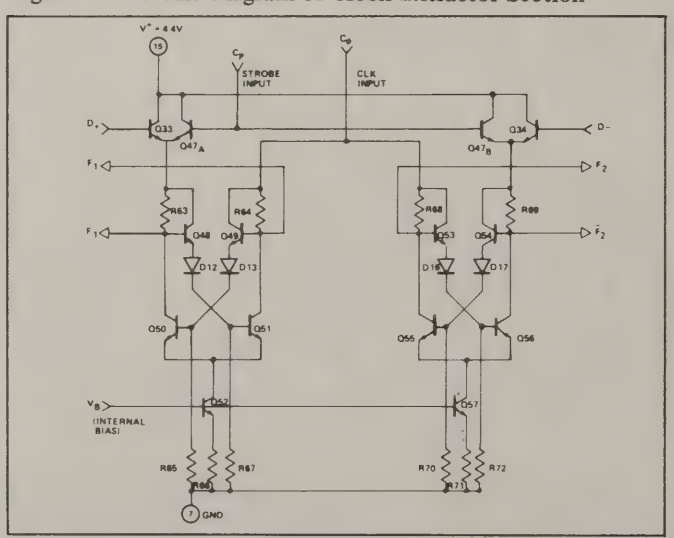


Figure 11. Data-Latch Section of XR-C277

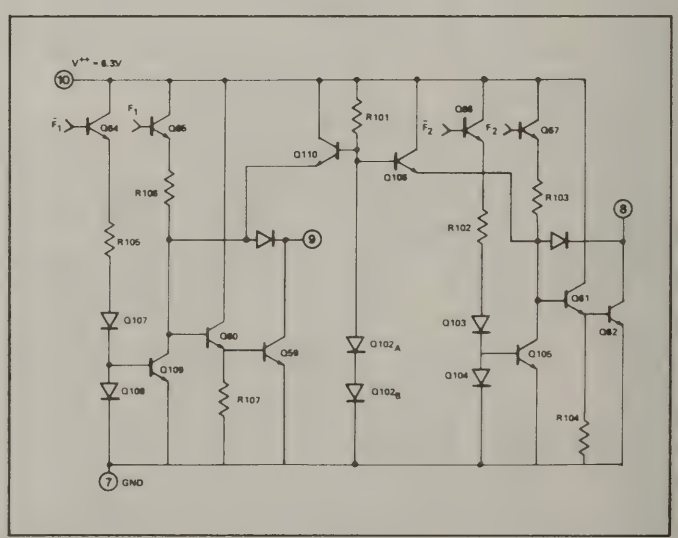


Figure 12. Output-Driver Section

Figure 13 shows the typical timing sequence of the circuit waveforms. For illustration purposes, a "one-zero-one" input data pattern is assumed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Storage Temperature Range	-65°C to +150°C

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-C277	CERDIP	-40°C to +85°C

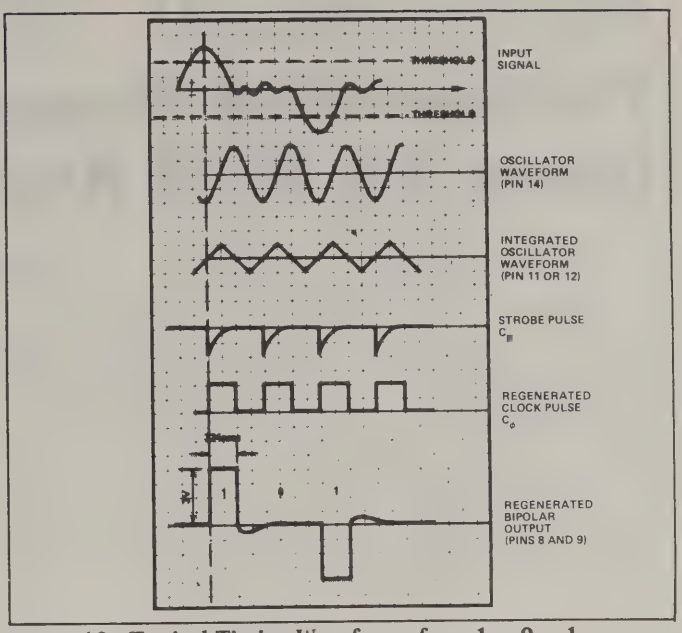


Figure 13. Typical Timing Waveforms for a 1 – 0 – 1 Input Data Pattern

ELECTRICAL CHARACTERISTICS

(–40° to +85°C, V++ = 6.3V ±0.5V, V+ = 4.4V ±0.15V, unless specified otherwise.)

PARAMETER	LIMITS				CONDITIONS
	MIN.	TYP.	MAX.	UNITS	
Supply Current					See Figure 4
I_A		3.5		mA	Measured at Pin 10
I_B		7.5		mA	Measured at Pin 15
Total Current	8	11	13	mA	$(I_C + I_B)$
Preamplifier					See Figure 7
Input Offset Voltage		1.5	15	mV	Measured at Pins 2 and 3
Input Bias Current		0.3	4	μA	Measured at Pins 2 and 3
Voltage Gain	44	48	51	dB	Single-ended gain
Preamp Output Swing					Measured at Pins 4 and 5
High Swing	3.45	3.6	3.75	V	Maximum voltage swing
Low Swing	1.25	1.4	1.55	V	Minimum voltage swing
Output DC Level	2.47	2.55	2.72	V	
ALBO Section					See Figure 8
ALBO "Off" Voltage		10	75	mV	Measured from Pin 1 and Pin 16 to ground
ALBO "On" Voltage	0.6	0.87	1.1	V	Measured at Pin 1
ALBO "On" Voltage	1.2	1.5	2.1	V	Measured at Pin 16
ALBO Threshold	1.35	1.50	1.65	V	Measured differentially across Pins 4 and 5
Differential Threshold	-75		+75	mV	Threshold difference for polarity reversal at Pins 4 and 5
ALBO "On" Impedance		5	10	Ω	Measured at Pin 1
ALBO "Off" Impedance	20	50		kΩ	Measured at Pin 1
Comparator Thresholds					See Figure 9
Clock Threshold	68	73	78	%	% of ALBO threshold
Data Threshold	47	50	53	%	% of ALBO threshold
Clock Extractor					See Figure 10
Oscillator Current	10	14	20	μA	@ +25°C
Tank Drive Impedance		50		kΩ	
Recommended OSC. Q	100				
$I_{injection}/I_{OSC.}$	6.5	7	7.5		Ratio of current in Q_{1B} to current in Q_{1A}
Output Driver					See Figure 12
Low Output Voltage	0.65	0.75	0.95	V	Measured at Pins 8 and 9, I_L = 15 mA
Output "Off" Current		5	100	μA	V_{out} = 20V
Output Pulse					See Figure 13
Maximum Pulse Width Error			±30	n sec	
Rise Time			80	n sec	
Full Time			80	n sec	

Application Note AN-05

Tri-State FSK Modem Design Using XR-2207 And XR-2211

INTRODUCTION

This application note describes the design principle and the operation of "tri-state" frequency-shift keyed (FSK) Modems for industrial process control systems. Compared to conventional "bi-state" Modems which utilize only the *mark* and *space* frequencies, the tri-state Modems utilize a third frequency, called the "carrier signal", for additional command and control functions. This carrier-control feature allows each Modem system connected to a central processor (CPU) to be interrogated or activated, one at a time, without interference from the other Modem transmitters or receivers within the same system.

The design and operation of conventional bi-state FSK Modems using the XR-2206 modulator and the XR-2211 demodulator are covered in Exar's Application Note AN-01. This application note extends these basic concepts to the design of FSK modulators or demodulators with tri-state operation capability.

FUNDAMENTALS OF TRI-STATE OPERATION

In a wide variety of industrial process control applications, it is necessary to have a number of separate sensors and controllers activated by a centralized computer or processing unit (CPU). This can be achieved by operating a number of separate FSK modulator/demodulator (Modem) stations over a common set of telephone lines and address to them, one at a time, from the CPU. The simplified block diagram of such a process control system is shown in Figure 1. In many cases, such a process controlled system also makes use of the "distributed-intelligence" concept by employing a separate data acquisition system at each control station. Such an *intelligent* data acquisition system is normally made up of a microprocessor along with its A/D and D/A converter circuitry which interface with the sensors and the control machinery; and an FSK Modem which interfaces with the telephone wires going back to the central command unit, the CPU.

In such a complex process control system, the FSK Modem stations play a crucial role in interfacing the distributed control stations with the CPU. The Modem arrays are selectively "interrogated" by the CPU, one at a time, by operating them under so-called "carrier-control" mode, i.e., they are addressed or enabled only when a specific carrier-tone is sent out from the CPU.

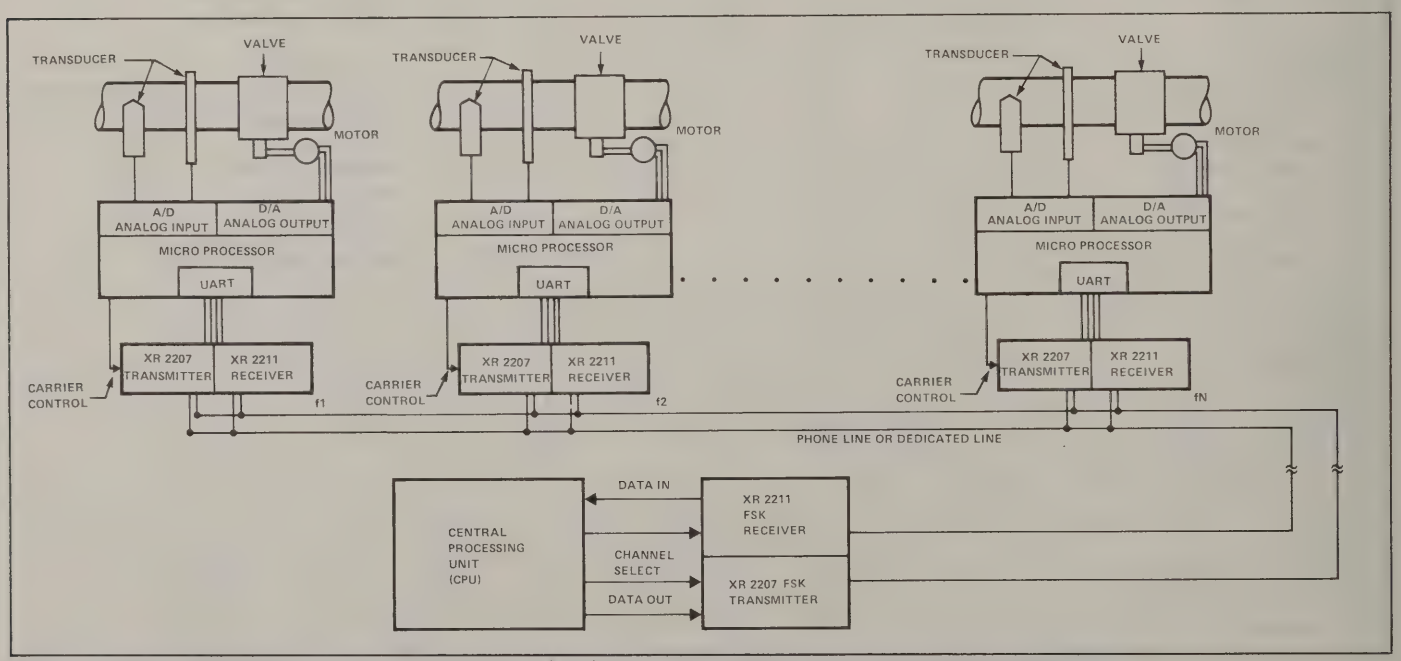


Figure 1. Simplified Block Diagram of a Complex Process Control System with multiple FSK Modems.

In conventional operation of FSK Modems, one operates them in their "bi-state" mode, i.e., the information to be transmitted or received is available in *two* states, corresponding to either a *mark* or a *space* frequency. In a complex process control system, such as the one shown in Figure 1, the versatility of the system can be greatly enhanced by operating the FSK modulator and the demodulator in a "tri-state" mode where the information to be transmitted or received is available in *three* states, i.e., a "mark" or a "space" frequency, or a "carrier" signal, which is normally a tone having a frequency half-way between the mark and space frequencies.

Figure 2 shows a detailed block diagram of a complete tri-state FSK Modem system. The system is made up of five blocks:

(A) FSK transmitter or encoder which converts the input data or logic signals into transmitted "mark", "space" and "carrier" tones.

(B) FSK receiver or decoder which converts the frequency signals sent over the telephone lines into binary logic signals.

(C) Transmitter band-pass filter which band-limits the frequency output of the transmitter to the allocated transmitter bandwidth.

(D) Receiver band-pass filter which limits the incoming signals to those frequencies which fall within the allocated receiver bandwidth.

(E) A "line hybrid", or a 4-wire to 2-wire transformer, which isolates or de-couples the transmitter output from the receiver input.

The first 2 blocks, i.e., the FSK transmitter and the receiver, are the essential part of the Modem system. The remaining three blocks, namely the active filters and the line-hybrid are support circuits, depending on the frequency-band requirements or the necessary telephone line interconnections. Detailed descriptions and design examples for these active filters are given in Exar's Application Note AN-03.

The tri-state Modem is designed to operate in two separate frequency bands: A "transmit-band" for the transmitted data, and a "receive-band" for the incoming frequencies. In certain operating modes, such as the half-duplex operation, these frequency bands may be one and the same. In its most general case, the frequency information associated with the tri-state Modem system of Figure 2, is concentrated in *three* discrete frequencies in each of the transmit- and receive-bands. These are:

Transmit-Band (transmitter output):

f_{T1} = Transmitter "mark" frequency

f_{T2} = Transmitter "space" frequency

f_{T0} = Transmitter "carrier" or "center" frequency

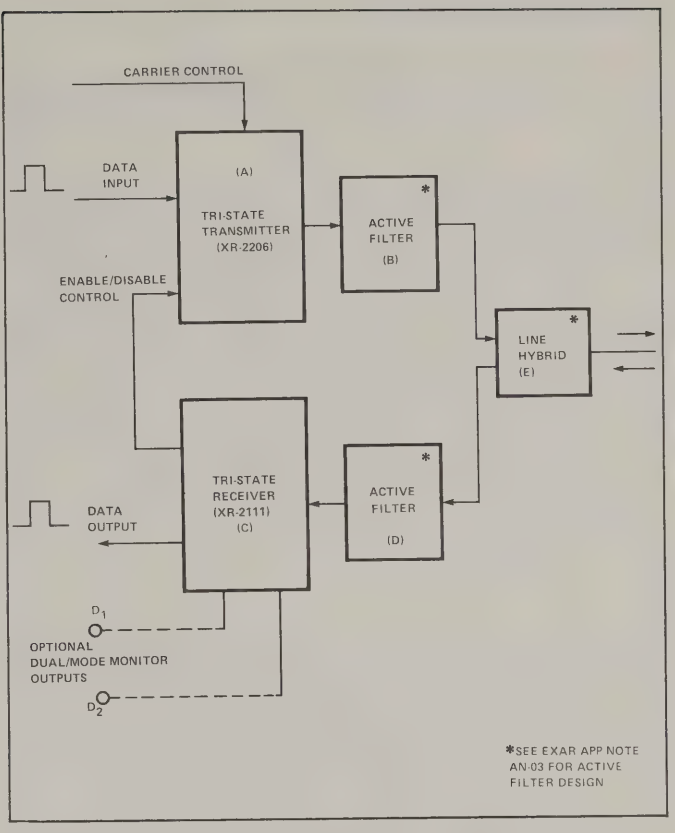


Figure 2. Block Diagram of a Tri-State FSK Modem System.

Receive-Band (receiver input):

f_{R1} = Receiver "mark" frequency

f_{R2} = Receiver "space" frequency

f_{R0} = Receiver "carrier" or "center" frequency

Normally the "mark" and "space" frequencies are chosen to be near the opposite edges of the receive- or transmit-band, and the "carrier" frequency is chosen to be at the center of the corresponding band.

When activated by the enable/disable control, the tri-state transmitter generates either the FSK mark/space frequencies (i.e., frequencies f_{T1} and f_{T2}) or the carrier frequency, f_{T0}. The carrier frequency is activated by the "carrier control" input, and can over-ride the input data.

The tri-state receiver provides two outputs: A binary data output, when activated by the input mark/space frequencies (i.e., f_{R1} and f_{R2}), and a logic signal to control or enable the transmitter, when the receive-carrier frequency, f_{R0}, is present. As an option, it may have a dual-mode operation capability which can provide serial data outputs for *half-bandwidth* deviations of the input signal, i.e., for FSK signals comprised of center-to-mark or center-to-space frequency shifts. The data outputs corresponding to this mode of operation are shown as outputs D_1 and D_2 of Figure 2.

MODES OF OPERATION

The generalized tri-state Modem system of Figure 2 can operate in a multiplicity of modes. Some of these are outlined below:

Answerback Under CPU Control: The Modem will be in a stand-by mode, with the transmitter disabled, and with the receiver in a stand-by condition with its data output disabled. It will be activated only when an "interrogate" tone at the receiver center frequency, f_{R0}, is transmitted by the control Modem unit associated with the CPU (see Figure 1). This tone is detected by the receiver; it activates the transmitter via its enable/disable control and instructs the local microprocessor to transmit its status information, via the local transmitter. This data is transmitted as an FSK signal made up of the transmit mark and space frequencies, f_{T1} and f_{T2}. When the information transmission is complete, or when the "interrogate" tone is discontinued, the entire Modem system again reverts back to its stand-by mode.

Receive Under CPU Control: In this mode of operation, the transmitter remains disabled, the receiver is at its stand-by mode with its data output disabled. When the FSK data is sent by the CPU Modem transmitter, at mark/space frequencies of f_{R1} and f_{R2}, the data output is enabled and the decoded binary data is fed into the local microprocessor. Since the "center" receive-frequency, f_{R0} is not transmitted, the transmitter remains disabled.

Priority-Transmit Request: In an "emergency" situation, the local transmitter can be activated, by its carrier-control input, which causes it to transmit a tone, f_{T0}, at its center frequency. When this tone is received by the CPU, it will be treated as a priority-request to transmit information; and the CPU will immediately "interrogate" the corresponding local Modem by sending out its address tone, at frequency f_{R0}.

Dual-Channel Receive: As an option, the receiver can provide serial data outputs, through separate terminals D_1 and D_2 of Figure 2, for half-bandwidth deviations of the input FSK signal. In this mode, the input data will be in the form of center-to-mark frequency shifts for one channel, and center-to-space shifts for the other. This mode of operation allows two separate sets of data or control instructions to be transmitted within the same channel bandwidth, provided that only one of these channels is used at any one time.

Dual-Channel Transmit: As an option, the transmitter can also transmit two separate channels, using half-bandwidth deviations of the transmit signal. In this case, the outgoing data will be encoded with center-to-mark transitions of the transmitter frequency in one of the channels; and with the center-to-space transitions in the other. However, similar to the case of the receiver, only one or the other, and not both, of these half-bandwidth channels can be "on" at a given time.

XR-2207 AS A TRI-STATE FSK TRANSMITTER

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) circuit with excellent temperature stability. It provides simultaneous triangle and square wave outputs and can be keyed to any one of *four* pre-programmed frequencies, by means of external logic signals. These four discrete frequencies are pre-programmed by the choice of four external timing resistors.

Figure 3 shows a functional block diagram of the XR-2207 monolithic FSK generator chip. The circuit is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and square wave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals.

The frequency of oscillation is set by an external timing capacitor, and by the combination, of one or more, of the external

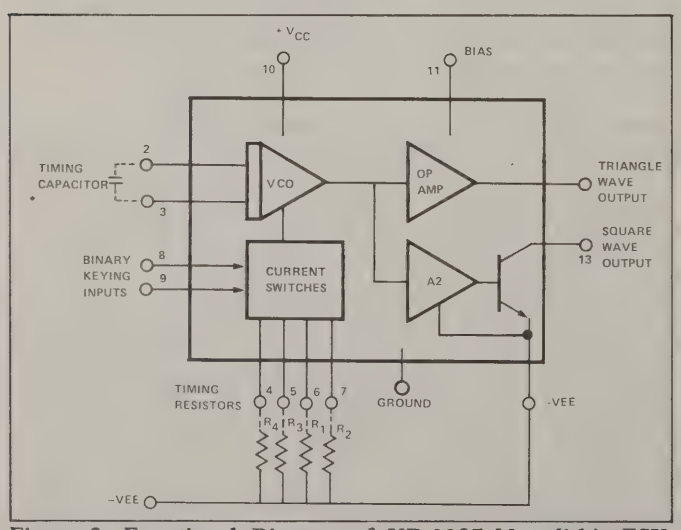


Figure 3. Functional Diagram of XR-2207 Monolithic FSK Generator.

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pins 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pins 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

TABLE 1. Output Frequency of the XR-2207 as a function of the Keying Logic.

(*Frequency in Hz, R in Ohms and C in Farads.)

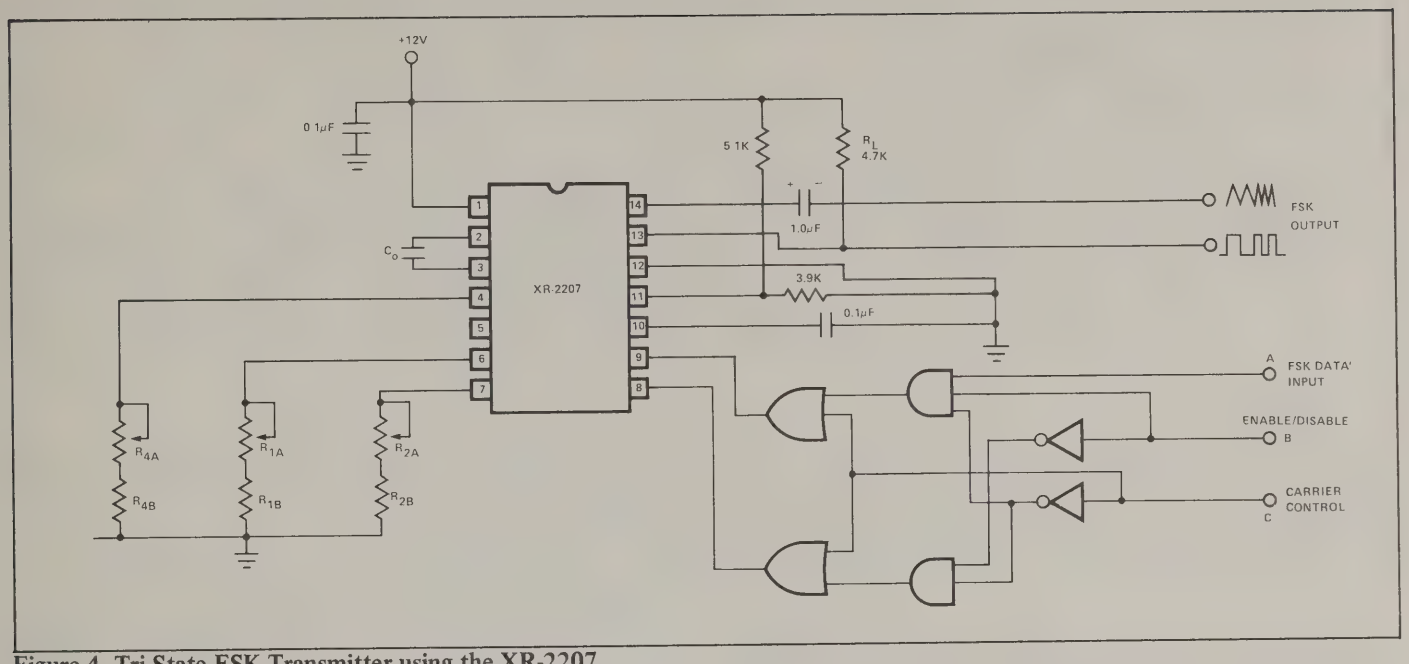


Figure 4. Tri-State FSK Transmitter using the XR-2207.

timing resistors, R_1 through R_4. The keying terminals switch these external resistors in and out of the circuit and thus, control the operating frequency. Table 1 shows the *four* discrete frequencies which can be obtained as a function of *four* logic states at pins 8 and 9. It should be noted that the frequency is inversely proportional to the timing resistor connected to the *activated* timing pin. Thus, for example, if only one of the timing pins, say pin 5, is activated, yet its associated resistor, R_3 is left open-circuited (i.e., $R_3 = \infty$) the oscillator will be keyed "off" since this corresponds to a "zero-frequency" state.

Figure 4 shows the recommended circuit connection of the XR-2207 for its operation as a tri-state FSK transmitter. The three resistors, R_1, R_2 and R_4 are used to set the three discrete frequencies to be transmitted in accordance with the frequency expressions given in Table 1, where:

$$f_{T1} = \frac{1}{C_0 R_1} \qquad f_{T2} = \frac{1}{C_0 R_1} + \frac{1}{C_0 R_2} \qquad f_{T0} = \frac{1}{C_0 R_4}$$

It should be noted that pin 5 is left open circuited (i.e., $R_3 = \infty$). This allows the circuit to be keyed "off", or disabled, by applying a "high" logic state to pin 8 and a "low" logic state to pin 9 (see Table 1).

The functions of the three control terminals can be described as follows:

A. **FSK Data Input**: The serial binary data is applied to this terminal. With the carrier control at "low" and Enable/Disable control at "high" state, the binary data causes the transmitter to generate the *mark* and *space* frequencies, f_{T1} and f_{T2}.

B. **Enable/Disable Control**: When this input is at "low" state, the transmitter is disabled.

C. **Carrier-Control**: When this terminal is at "high" state, the transmitter generates a continuous tone at frequency f_{T0}.

With the external logic circuitry as shown in Figure 4, Carrier-Control can over-ride both the Enable/Disable or the FSK data inputs. A detailed truth-table of the circuit outputs is given in Table 2, for various states of the three control inputs.

XR-2211 AS A TRI-STATE RECEIVER

The XR-2211 is a monolithic FSK demodulator which operates on the phase-locked loop principle. In addition to the basic PLL system, the monolithic chip also contains a quadrature-detector circuit which produces a logic signal when a carrier signal, or tone, is present within the capture range of the PLL. A simplified functional block diagram of the circuit is shown in Figure 5.

Basic Bi-State Operation: The basic operation of the XR-2211, in conventional bi-state Modems, is described in detail in

CONTROL INPUT STATES			LEVEL AT PIN 9	LEVEL AT PIN 9	TRANSMITTER OUTPUT FREQUENCY	TRANSMITTER OPERATING MODE
A	B	C				
L	L	L	L	H	OFF	TRANSMITTER OFF
H	L	L	L	H	OFF	
L	H	L	L	L	f_{T1}	TRANSMIT DATA
H	H	L	H	L	f_{T2}	
L	L	H	H	H	f_{T0}	TRANSMIT CARRIER ONLY
L	H	H	H	H	f_{T0}	
H	H	H	H	H	f_{T0}	

TABLE 2. Tri-State Transmitter Operating Modes as a function of Control Inputs.

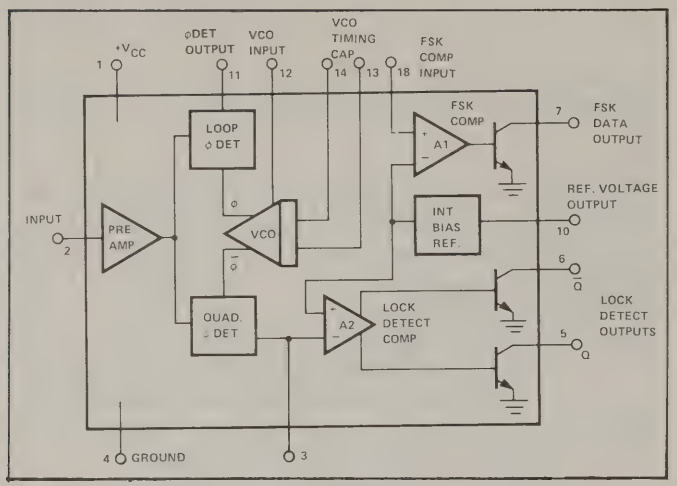


Figure 5. Functional Block Diagram of XR-2211 FSK and Tone Detector.

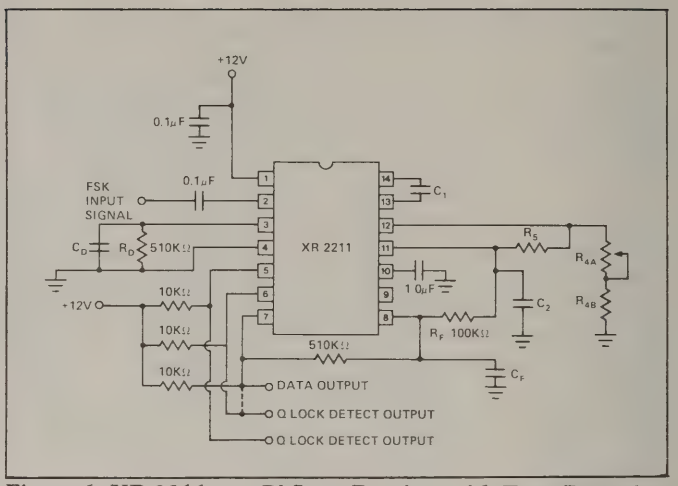


Figure 6. XR-2211 as a Bi-State Receiver with Tone-Detection Capability.

Exar's Application Note AN-01. It will be briefly reviewed below:

The basic circuit connection for the XR-2211 for bi-state FSK detection is shown in Figure 6. The center frequency is determined by $f_0 = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. f_0 should be calculated to fall midway between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula:

$$\Delta f = (R_4 f_0/R_5)\ \text{Hz}.$$

Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability the recommended range of values for R_4 is between 10 kΩ and 100 kΩ.

The capture range ($\pm\Delta f_c$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop filter time constant. In most Modem applications, Δf_c is chosen to be ≈ 80% to 95% of the tracking range, Δf.

The bi-state FSK data filter, made up of R_F and C_F removes the jitter from the demodulated FSK signal. Similarly, the lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510 kΩ, the minimum value of C_D can be determined by: C_D (μf) ≈ 16/capture range in Hz. The XR-2211 has three NPN open collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, pin 5 is the Q lock-detect output, which goes low when a carrier is detected, and pin 6 is the $\bar{Q}$ lock-detect output, which goes high when lock is detected. If pins 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied and will be "low" when no carrier is present.

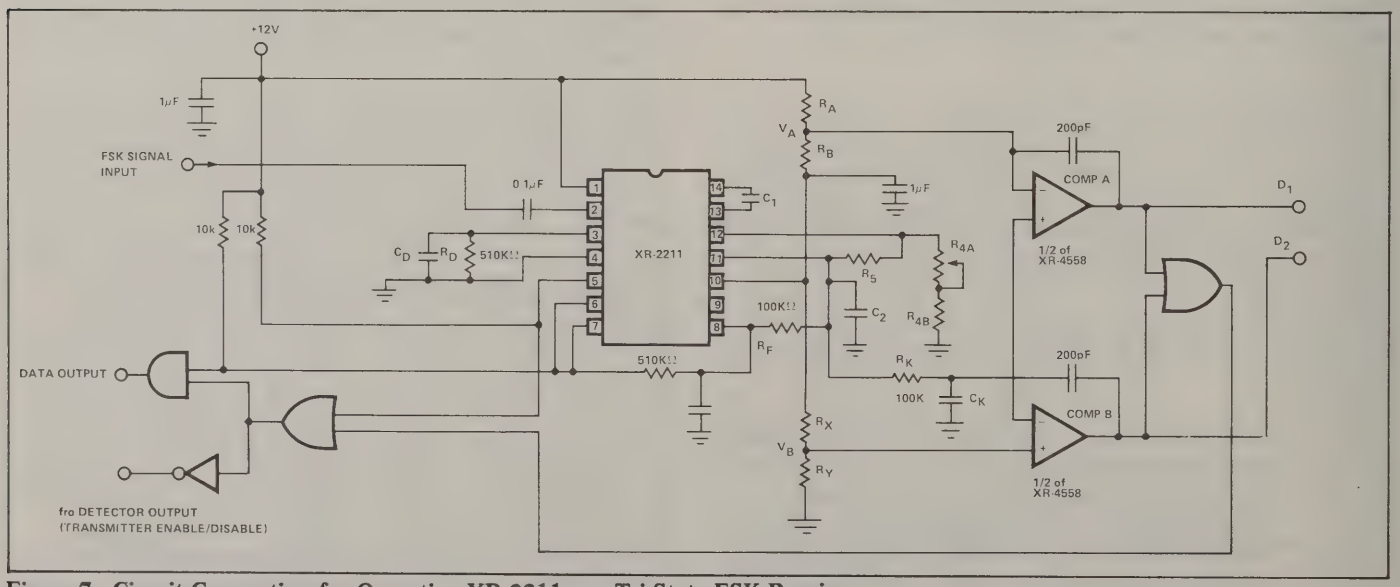


Figure 7. Circuit Connection for Operating XR-2211 as a Tri-State FSK Receiver

Tri-State Operation: The XR-2211 FSK demodulator circuit can be made to operate as a tri-state receiver (see Block B of Figure 2) using the circuit configuration shown in Figure 7. With reference to the Figure, the basic operation of the circuit can be described as follows:
The basic FSK decoding function, i.e., converting the incoming "mark" and "space" signals at frequencies f_{R1} and f_{R2}, is performed in the same manner as in the bi-state case and the resulting output is available at pin 7 of XR-2211. Pin 7 is connected to the tone-detect output, and then gated by the complement of the carrier-detect output. Thus, the "Data Output" terminal will be enabled only when the mark and space frequencies are present, but *not* when the receive-carrier, f_{R0}, is present.

The external voltage comparators shown in Figure 7 are added to the circuit to distinguish PLL output voltage levels corresponding to various input frequencies. Their function can be understood by referring to Figure 8, which shows the XR-2211 frequency-to-voltage transfer characteristics, at pin 11. The voltage levels and polarities shown are relative to the XR-2211 internal reference voltage, V_{10}, at pin 10. The mark and space frequencies, f_{R1} and f_{R2}, generate the maximum d-c level shifts V_{R1} and V_{R2}, that are sensed by the internal FSK comparator (see Figure 5) which is internally biased from the reference voltage, V_{10}.

The external comparators, Comp. A and Comp. B of Figure 7, are biased at voltage levels V_A and V_B, at approximately half-way between V_{R1} and V_{R2}, to trip at frequencies f_A and f_B, which are half-way between mark-to-center and space-to-center frequency shifts. This biasing is achieved with the external resistive dividers, R_A, R_B, R_X and R_Y of Figure 7, which generate the reference voltage levels, V_A and V_B, with respect to the XR-2211 internal reference at pin 10. It should be noted that the values of the resistors, $(R_A + R_B)$ and $(R_X + R_Y)$ must be as large as possible (typically in excess of 100 kΩ) to avoid disturbing the voltage level at pin 10.

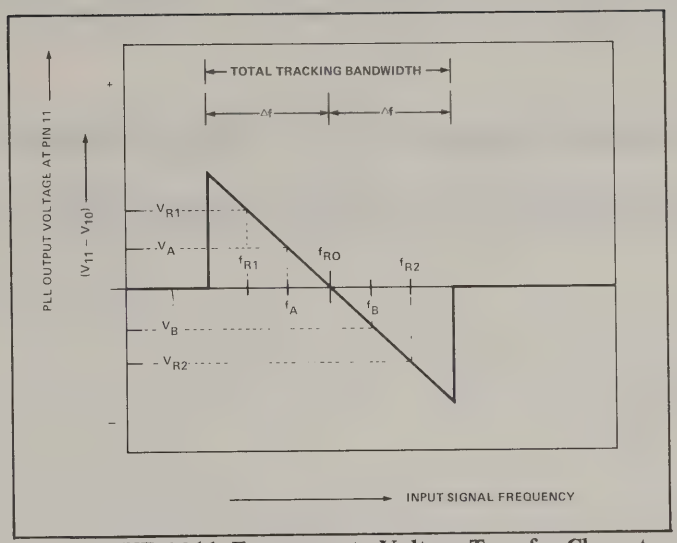


Figure 8. XR-2211 Frequency-to-Voltage Transfer Characteristics. (Note: V_{11} and V_{10} are the DC voltage levels at pins 11 and 10, respectively.)

The output of pin 11 is filtered by R_K and C_K and is used to drive the external voltage comparators. The outputs of these comparators are then connected through the external logic gates, to produce the carrier-detect or the enable/disable signal. The resulting logic output will be normally at a "low" state, and will go "high" only when the carrier signal, f_{R0}, is present. This logic signal is normally used for transmitter enable/disable control, as shown in Figure 2.

The logic level changes at external comparator outputs correspond to mark-to-carrier or space-to-carrier frequency shifts (see Figure 8); thus, these outputs can be utilized as optional "Dual-Mode Monitor" outputs, D_1 and D_2, of Figure 2.

Application Note AN-06

Precision PLL System Using the XR-2207 and the XR-2208

INTRODUCTION

The phase-locked loop (PLL) is a versatile system block, suitable for a wide range of applications in data communications and signal conditioning. In most of these applications, the PLL is required to have a highly stable and predictable center frequency and a well-controlled bandwidth. Presently available monolithic PLL circuits often lack the frequency stability and the versatility required in these applications.

This application note describes the design and the application of two-chip PLL system using the XR-2207 and the XR-2208 monolithic circuits. The XR-2207 is a precision voltage controlled oscillator (VCO) circuit with excellent temperature stability (±20 ppm/°C, typical) and linear sweep capability. The XR-2208 is an operational multiplier which combines a four quadrant multiplier and a high gain operational amplifier in the same package. Both circuits are designed to interface directly with each other with a minimum number of external components. Their combination functions as a high performance PLL, with the XR-2207 forming the VCO section of the loop, and the XR-2208 serving as the phase-detector and loop amplifier.

As compared with the presently available single-chip PLL circuits such as the XR-210 or the Harris HI-2820, the two-chip PLL system described in this paper offers approximately a factor of 10 improvement in temperature stability and center frequency accuracy. The system can operate from 0.01 Hz to 100 kHz, and its performance characteristics can be tailored to given design requirements with the choice of only four external components.

DEFINITIONS OF PLL PARAMETERS

The phase-locked loop (PLL) is a unique and versatile feedback system that provides frequency selective tuning and filtering without the need for coils or inductors. It consists of three basic functional blocks: phase comparator, low-pass filter, and voltage-controlled oscillator, interconnected as shown in Figure 1. With no input signal applied to the system, the error voltage, V_d, is equal to zero. The VCO operates at a set "free-running" frequency, f_o. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input signal frequency, f_s, is sufficiently close to f_o, feedback causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

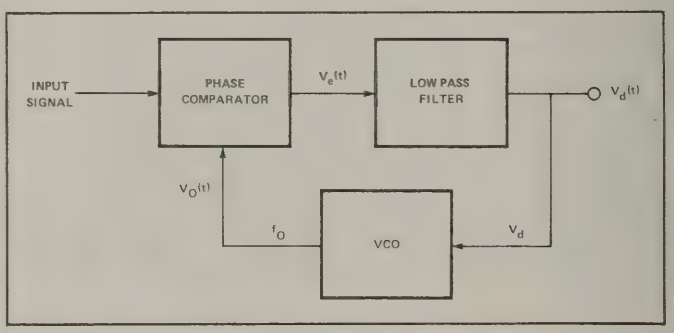


Figure 1. Block Diagram of a Phase-Locked Loop.

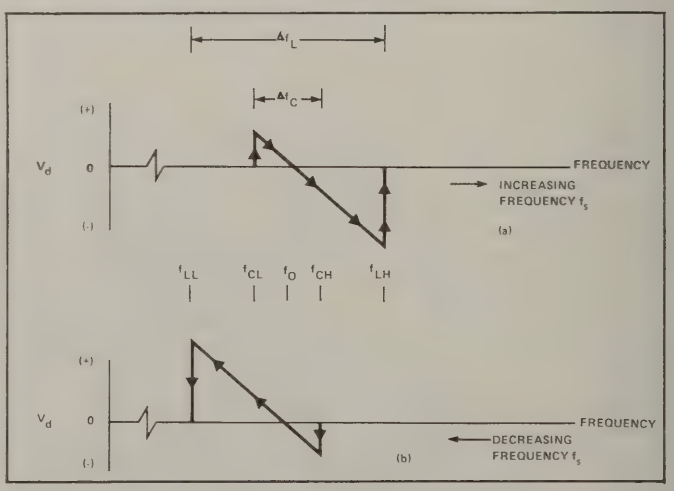


Figure 2. Frequency to Voltage Transfer Characteristics of a PLL System; (a) Increasing Input Frequency; (b) Decreasing Input Frequency.

Two key parameters of a phase-locked loop system are its "lock" and "capture" ranges. These can be defined as follows:

Lock Range = The band of frequencies in the vicinity of f_o over which the PLL can *maintain lock* with an input signal. It is also known as the "tracking" or "holding" range. Lock range increases as the overall loop gain of the PLL is increased.

Capture Range = The band of frequencies in the vicinity of f_o where the PLL can *establish* or *acquire lock* with an input signal. It is also known as the "acquisition" range. The capture is always smaller than the lock range. It is related to the low pass filter bandwidth and decreases as the low pass filter time constant increased.

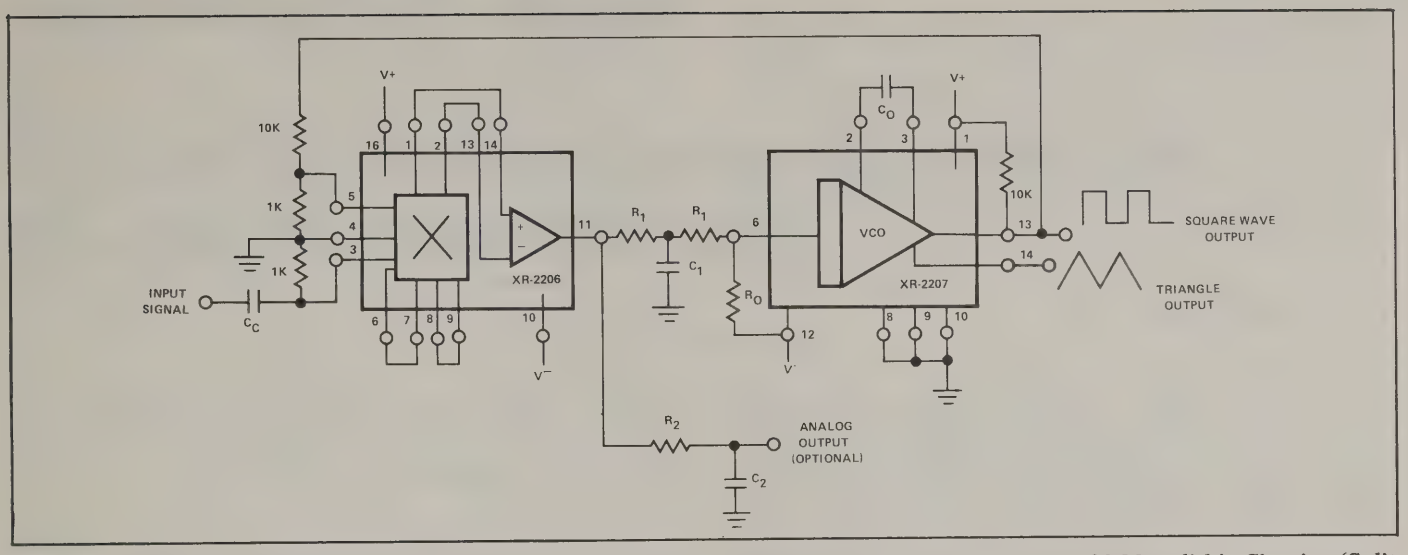


Figure 3. Circuit Interconnections for the Precision PLL System Using the XR-2207 and the XR-2208 Monolithic Circuits. (Split-Supply Operation, ±6V to ±13V.)

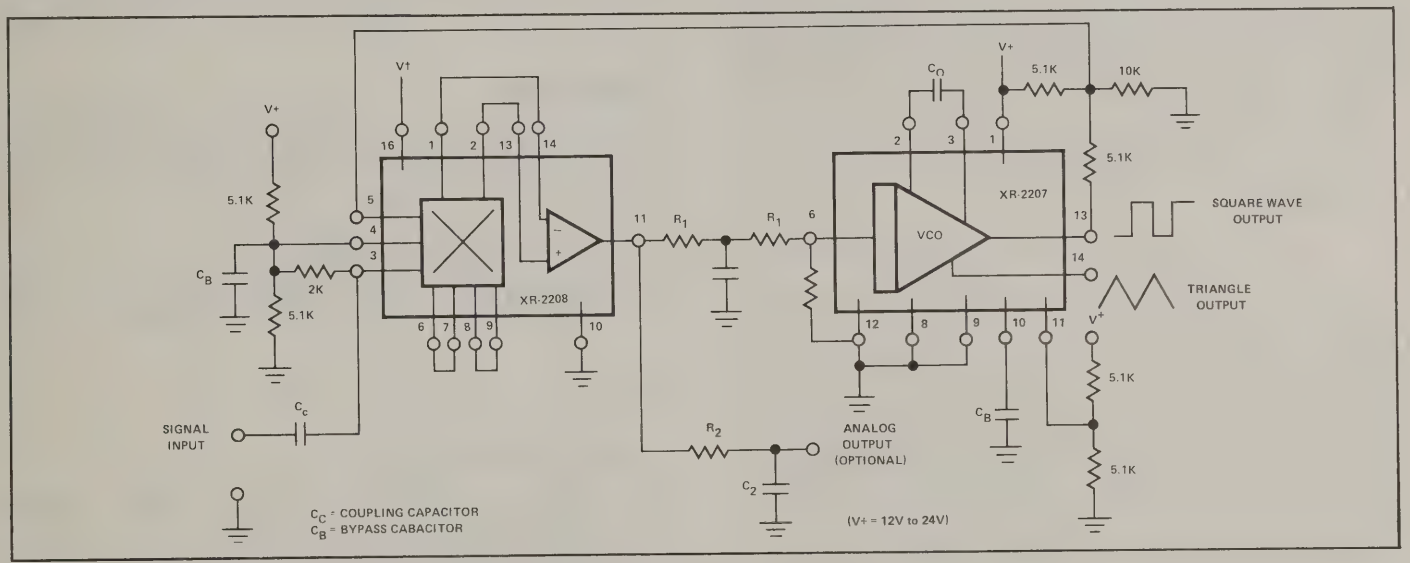


Figure 4. Circuit Interconnections for Single Supply Operation.

TABLE 1

Phase-Locked Loop Design Equations*

(1) Center Frequency: $f_o = \frac{1}{R_0 C_0}$ Hz

(2) Lock Range: $(\Delta f_L / f_0) = (0.9)(R_0/R_1)$

(3) Phase Detector Gain: $K_\phi = 0.5\ V_{cc}$ volts/radian
Where $V_{cc} = V^+$ for split supply; $V_{cc} = V^+/2$ for single supply.

(4) VCO Conversion Gain: $K_v = \frac{1}{2\ V_{cc} C_0 R_1}$ rad/sec/volt

(5) Loop Gain: $K_L = K_\phi K_v = \frac{0.25}{C_0 R_1}$ sec^{-1}

(6) Low Pass Filter Time Constant: $\tau = \frac{C_1 R_1}{2}$ sec.

(7) Loop Damping: $= \frac{1}{2\sqrt{\tau K_L}} = \sqrt{\frac{2\ C_0}{C_1}}$

(8) Capture Range:

a) Underdamped Loop ($\xi < 1/2$):

$$(\Delta f_c / f_0) = \frac{0.8 R_0}{R_1} \sqrt{\frac{C_0}{C_1}}$$

b) Overdamped Loop ($\xi > 1$):

$$(\Delta f_c / f_0) = 0.8(R_0/R_1)$$

*See Figures 3 and 4 for component designation.

The PLL responds only to those input signals sufficiently close to the VCO frequency, f_0, to fall within the "lock" or "capture" ranges of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about f_0. Figure 2 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly, over a broad frequency range covering both the "lock" and the "capture" ranges of the PLL. The vertical scale corresponds to the filtered loop error voltage, V_d, appearing at the VCO control terminal.

As the input frequency, f_s, is swept up (Figure 2(a)) the system does not respond to the input signal until the input frequency reaches the lower end of capture range, f_{CL}. Then, the loop suddenly locks on the input signal, causing a positive jump in the error voltage V_d. Next, V_d varies at a slope equal to the reciprocal of VCO voltage-to-frequency conversion gain, (K_v), and goes through zero at $f_s = f_0$. The loop tracks the input frequency until f_s reaches the upper edge of the lock range, f_{LH}. Then the PLL loses lock, and the error voltage drops to zero. If the input frequency is swept back slowly, from high towards low frequencies the cycle repeats itself, with the characteristics shown in Figure 2(b). The loop captures the signal at the upper edge of the capture range, f_{CH}, and tracks it down the lower edge of the lock range, f_{LL}. With reference to the figure, the "lock" and the "capture" ranges can be defined as:

$$\text{Lock Range} = \Delta f_L = f_{LH} - f_{LL}$$

$$\text{Capture Range} = \Delta f_C = f_{CH} - f_{CL}$$

The gain parameters associated with the PLL are defined as follows:

Phase Detector Gain, $K\phi$: Phase detector output per unit of phase difference between the two signals appearing at the phase detector inputs. It is normally measured in volts per radian.

VCO Conversion Gain, K_v: VCO frequency change per unit of input voltage. It is normally measured in radians/sec./volt.

Loop Gain, K_L: Total d_c gain around the feedback loop. It is equal to the product of $K\phi$ and K_v.

Loop Damping Factor, ζ: Defines the response of the loop error voltage V_d, to a step change in frequency. If $\zeta < 1$, the loop is underdamped; and the error voltage V_d will exhibit an underdamped response for a step change of signal frequency.

The lock range of the phase-locked loop is controlled by the loop gain, K_L. The capture range and the damping factor are controlled by both the loop gain and the low pass filter.

PRECISION PLL USING XR-2207 AND XR-2208

The XR-2207 VCO and the XR-2208 operational multiplier can be inter-connected as shown in Figure 3, to form a highly stable PLL system. The circuit of Figure 3 operates with supply voltages in the range of ±6 volts to ±13 volts; and over a frequency range of 0.01 Hz to 100 kHz. In the PLL system of Figure 3, all the basic performance characteristics of the PLL can be controlled and adjusted by the choice external 4 components identified as resistors R_0 and R_1, and the capacitors C_0 and C_1, C_0 and R_0 control the VCO center frequency; R_1 and C_1 determine the tracking range and the low pass filter characteristics. The two-chip PLL system can be readily converted to single supply operation by inter-connecting the circuit as shown in Figure 4. The PLL circuit of Figure 4 operates over a supply voltage range of +12V to +26V.

For best results, the timing resistor R_0 should be in the range of 5k to 100k, and $R_1 > R_0$. Under these conditions, the basic parameters of the PLL can be easily calculated from the design equations listed in Table 1.

Design Example

As an example, consider the design of a PLL system using the circuit of Figure 3, to meet the following nominal performance specifications:

a) Center Frequency = 10 kHz
b) Tracking Range = 20% (9 kHz to 11 kHz)
c) Capture Range = 10% (9.5 kHz to 10.5 kHz)

Solution:

a) Set Center Frequency:
Choose $R_0 = 10k$ (Arbitrary choice for $5k < R_0 < 100k$)
Then, from equation 1 of Table 1:
$C_0 = (1/f_0R_0) = 0.01\ \mu F$

b) Set Lock Range:
From equation 2 of Table 1:
$R_1 = (0.45)\ R_0 = 45k$

c) Set Capture Range:
Since capture range is significantly smaller than Lock range, equation 8(a) applies.
Solving equation 8(a) for C_1, one obtains:
$C_1 = 0.032\ \mu F$

Application Note AN-07

Single-Chip Frequency Synthesizer Employing the XR-2240

INTRODUCTION

The XR-2240 monolithic timer/counter contains an 8-bit programmable binary counter and a stable time-base oscillator in a single 16-pin IC package. Although the circuit was originally designed as a long-delay timer capable of generating time delays from microseconds to weeks, it also offers a wide range of other applications beyond simple time-delay generation. One such unique application is its use as a single-chip, frequency synthesizer, where it can generate over 2,500 discrete frequencies from a single reference frequency input.

PRINCIPLE OF OPERATION

The operation of the XR-2240 as a frequency synthesizer is possible because of the ability of the circuit to both *multiply* and *divide* the input frequency reference. It can, simultaneously, multiply the input frequency by a factor, "M," and divide it by a factor "N+1," where both M and N are adjustable integer values. Therefore, the circuit can produce an output frequency, f_O, related to the input reference frequency f_R as:

$$f_O = f_R \frac{M}{1+N}$$

Figure 1 shows the circuit connection for operating the XR-2240 timer/counter as a self-contained frequency synthesizer. The integer values M and N can be externally adjusted over a broad range:

$$1 \leqslant M \leqslant 10 \quad 1 \leqslant N \leqslant 255$$

The multiplication factor M is obtained by locking on the harmonics of the input frequency. The division factor N is determined by the pre-programmed count in the binary counter section. The principle of operation of the circuit can be best understood by briefly examining its capabilities for frequency division and multiplication separately.

Frequency Division by (1+N):

When there is no external reference input, f_R, the time-base oscillator section of the XR-2240 free-runs at its set frequency, f_S ($f_S = 1/RC$), where R and C are the external components at pin 13. The 8-bit binary counter can be programmed to divide the time-base frequency by an integer count, N, and generate an output pulse train whose frequency is:

$$f_O = f_S \frac{1}{1+N}$$

Frequency Multiplication by "M":

Frequency multiplication is achieved by synchronizing the time-base oscillator with the *harmonics* of the input sync or reference signal. Thus, if the time-base oscillator is made to free-run at "M" times the input frequency, it can be made to synchronize with the "M"th harmonic of the input reference signal. Typical capture range of the circuit is better than ±3%, for values of $1 \leqslant M \leqslant 10$; and since the time-base is accurate to within ±0.5% of the external R-C setting, lock-up does not present a problem for a given harmonic lock setting.

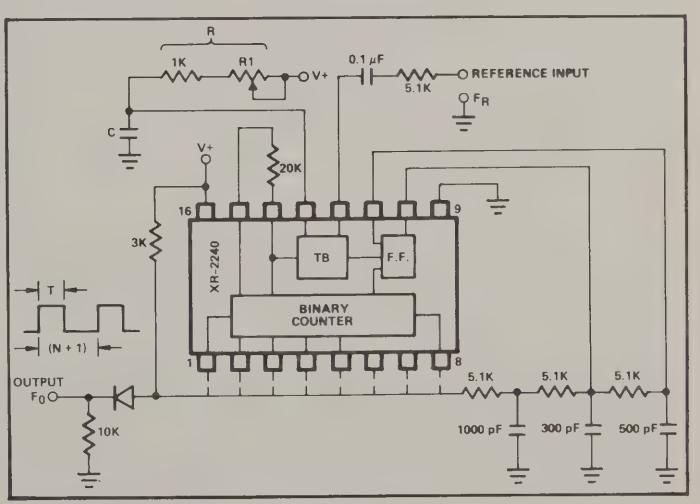


FIGURE 1

Circuit Operation:

With reference to Figure 1, the operation of the synthesizer circuit can be briefly explained as follows: The reference input frequency, f_R, is applied to the time-base sync terminal (pin 12) through a 5.1 KΩ series resistance and a coupling capacitor. The recommended waveform for the input frequency, f_R, is a 3 Vpp pulse train with a pulse width in the range of 30% to 80% of the time-base period, T. The multiplication factor M is chosen by the potentiometer R_1 which sets the time-base period T (T = RC). If no external reference is used, then M is automatically equal to 1.

The divider modulus, N, is chosen by shorting various counter outputs to a 3K common pull-up resistor. The output waveform is a pulse train with a fixed pulse width, T = RC, and a period $T_O = (N + 1)RC$.

The external R-C network between the output and the trigger and reset terminals of the XR-2240 is a non-critical delay network which resets and re-triggers the circuit to maintain a periodic output waveform. For the component values shown in Figure 1, the circuit can operate with the timing components R and C in the range of:

$$0.005\ \mu F \leqslant C \leqslant .1\ \mu F; 1\ K\Omega \leqslant R \leqslant 1\ M\Omega$$

The XR-2240 is a low-frequency circuit. Therefore, the maximum output frequency is limited to ≈200 kHz, by the frequency capability of the internal time base oscillator.

A particularly useful application of the simple synthesizer circuit of Figure 1 is to generate stable clock frequencies which are synchronized to an external reference, such as the 60 Hz line frequency. For example, one can generate a 100 Hz reference synchronized to 60 Hz line frequency simply by setting M = 5 and N = 2 such that:

$$f_O = f_R \frac{M}{1+N} = (60) \frac{5}{1+2} = 100\ Hz$$

Application Note AN-08

Dual Tone Decoding with XR-567 and XR-2567

INTRODUCTION

Two integrated tone decoders, XR-567 units, can be connected (as shown in Figure 1A) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R'_1C'_1$ are chosen, respectively, for tones 1 and 2. If sequential tones (1 followed by 2) are to be decoded, then C_3 is made very large to delay turn-off of unit 1 until unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 1B shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R_2 and CR_1 until activated by tone 1. A further variation is given in Figure 1C. Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn-on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

The XR-2567 Dual Tone Decoder can replace two integrated tone decoders in this application.

HIGH SPEED, NARROW BAND TONE DECODER

The circuit of Figure 1 may be used to obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70 mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_O$ and $1300/f_O$ mfd where f_O is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

TOUCH-TONE DECODER

Touch-Tone decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every tone. A low-cost decoder can be made as shown in Figure 2. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% of 100 mV and 5% at 50 mV rms. Capacitor C_4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltages (50 to 100 mV rms), the bandwidth can be controlled in the normal manner by selecting C_2, thereby eliminating the seven R_2 resistors and C_4. In this case, C_2 would be 4.7 mfd for the three lower frequencies or 2.2 mfd for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. As shown in the 567 data sheet under Alternate Method of Bandwidth Reduction, the external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R_2 resistors. In effect, the five 567's which are not being activated during the decoding process serve as bias voltage sources for the R_2 resistors of the two 567's which are being activated. Capacitor C_4 (optional) decouples the ac currents at the common point.

LOW COST FREQUENCY INDICATOR

Figure 3 shows how two tone decoders set up with overlapping detection bands can be used for a go/no/go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is set 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

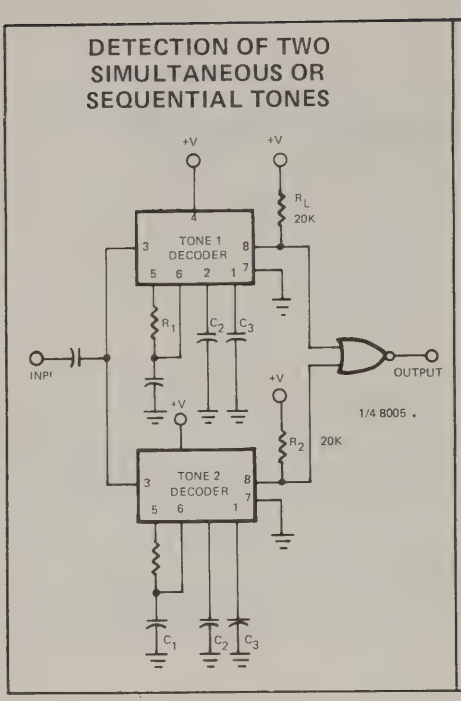


FIGURE 1A

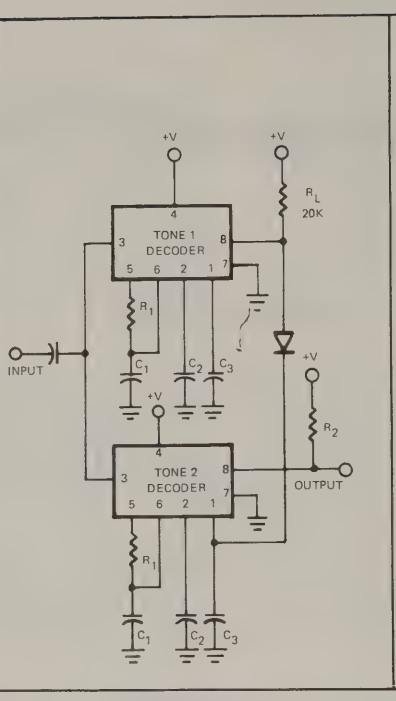


FIGURE 1B

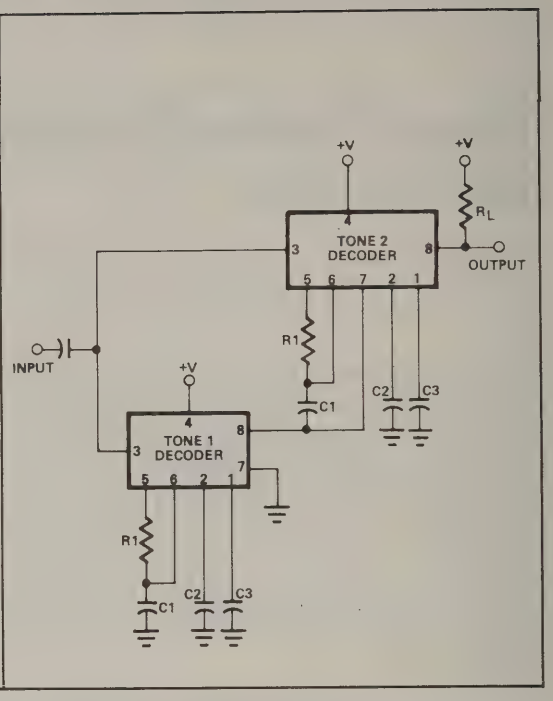


FIGURE 1C

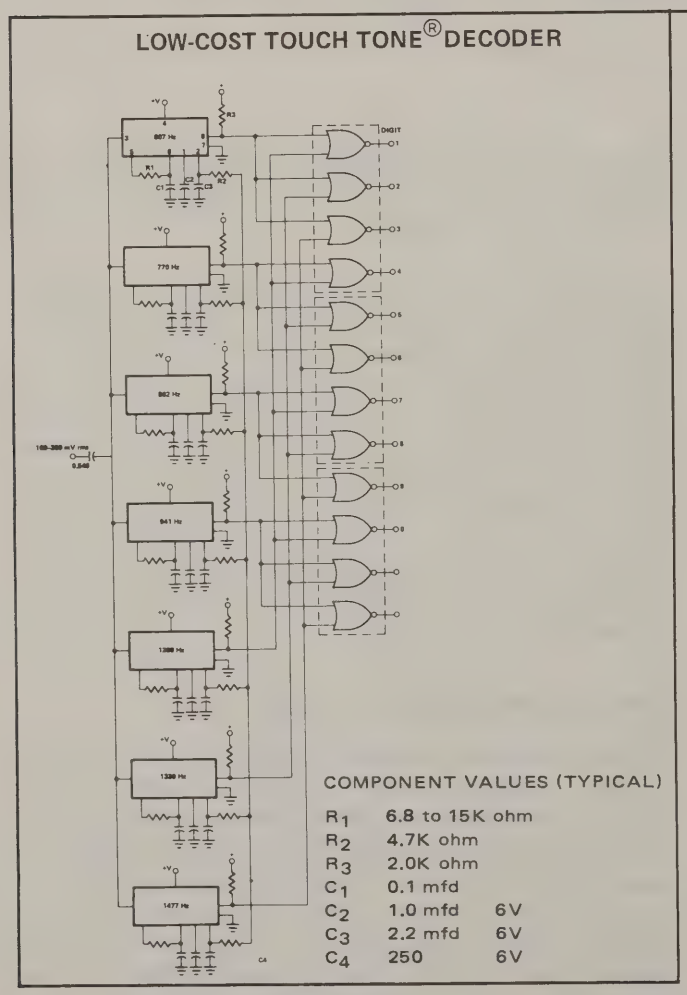


FIGURE 2

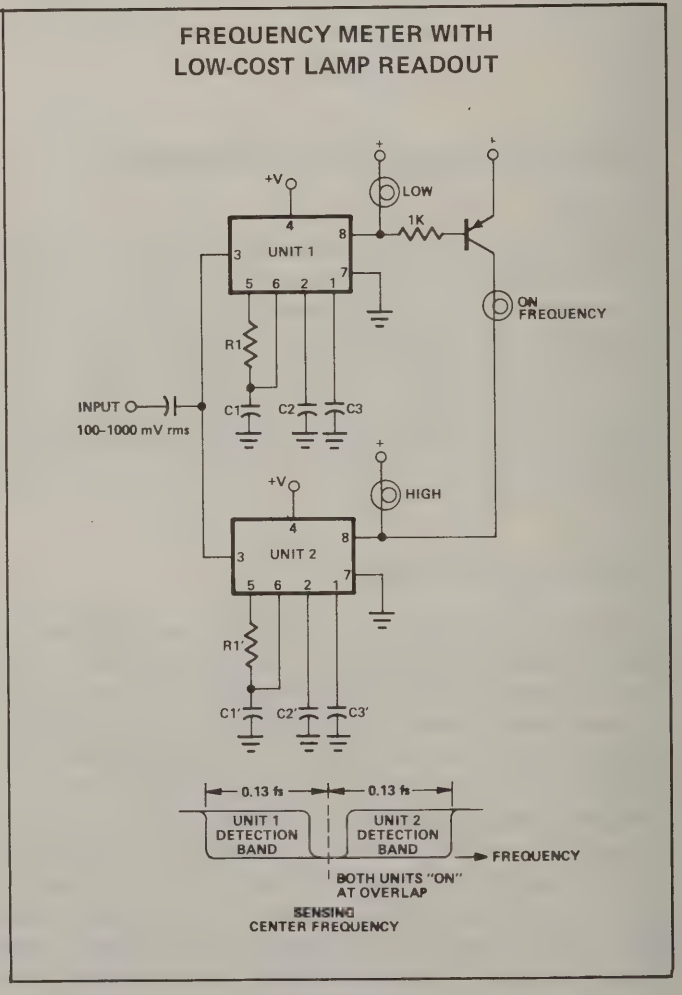


FIGURE 3

Application Note AN-09

Sinusoidal Output From XR-215 Monolithic PLL Circuit

INTRODUCTION

In a wide range of communication or signal conditioning applications, it is necessary to obtain a sinusoidal output signal which is synchronized to a desired reference or clock input. This can be achieved by using the XR-215 type monolithic PLL circuit and an additional sine-shaping network.

When a periodic input signal is present within the capture range of the XR-215 PLL, the system will "lock" on the input; and the VCO section of the PLL will synchronize with the input frequency. The output of the oscillator section of the PLL can then be converted to a low distortion sine wave by a relatively simple sine-shaping circuit.

PRINCIPLE OF OPERATION

Figure 1 contains a functional block diagram of the XR-215 monolithic PLL system. The circuit consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and a high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self-contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

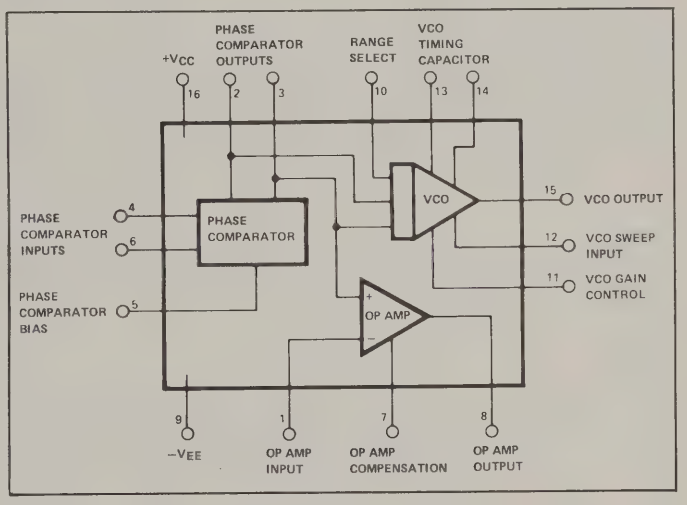


Figure 1. Functional Block Diagram of XR-215 Phase-Locked Loop

Figure 2 shows the simplified circuit schematic of the XR-215 phase-locked loop IC. The VCO part of XR-215, shown in the

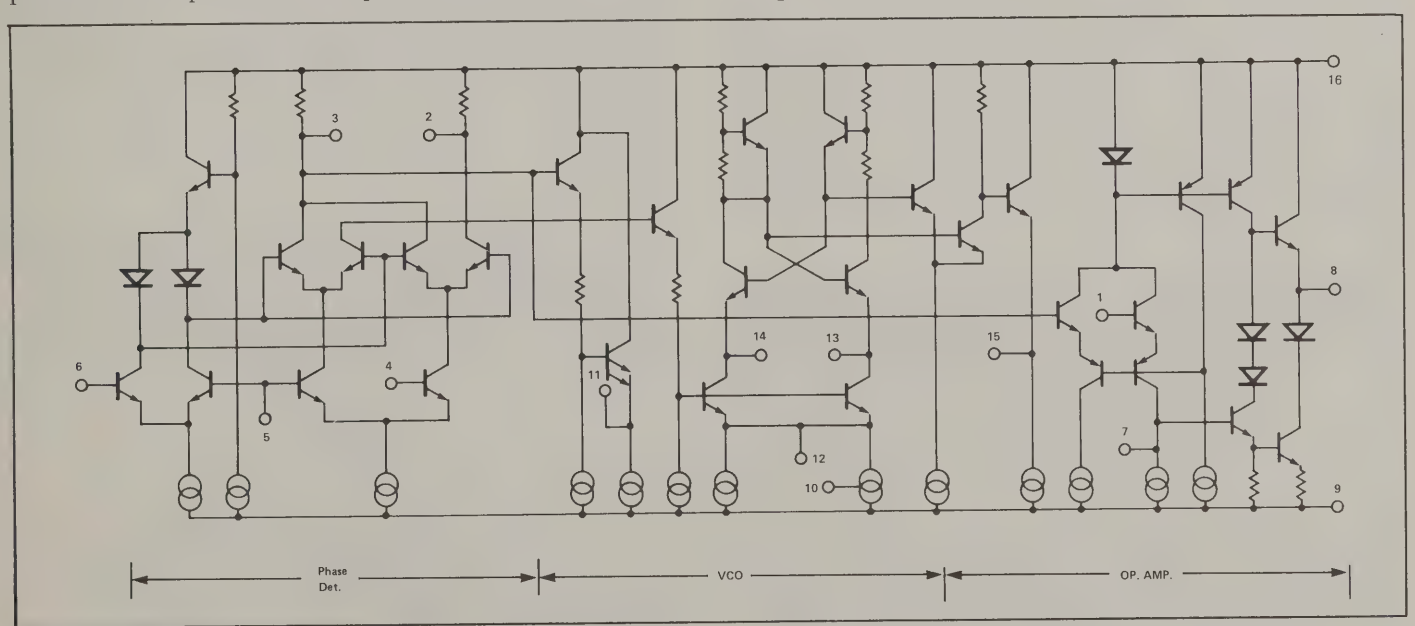


Figure 2. Simplified Circuit Schematic of XR-215

center section of Figure 2, is an emitter-coupled multivibrator circuit, whose frequency is set by an external capacitor, C_0, connected across the timing terminals (pins 13 and 14). In this type of an oscillator, the differential voltage waveform across the timing capacitor, C_0, is a linear triangle, with a peak-to-peak amplitude of 1.4 volts. This output amplitude across the timing capacitor is independent of supply voltage.

This triangular waveform can be shaped into a low distortion sinewave by passing it through a simple differential gain stage, as shown in Figure 3. By adjusting the potentiometer R_q of Figure 3, the input transistors T_1 and T_2 of the differential stage can be brought to the verge of cutoff at the positive and the negative extremities of the input triangle wave. This causes the peaks of the triangle waveform to be rounded, resulting in a nearly sinusoidal output waveform from the differential stage. If the transistor characteristics and the current levels in the differential gain stage are well matched, one can reduce the total harmonic distortion (THD) of the sinusoidal output waveform to less than 3%.

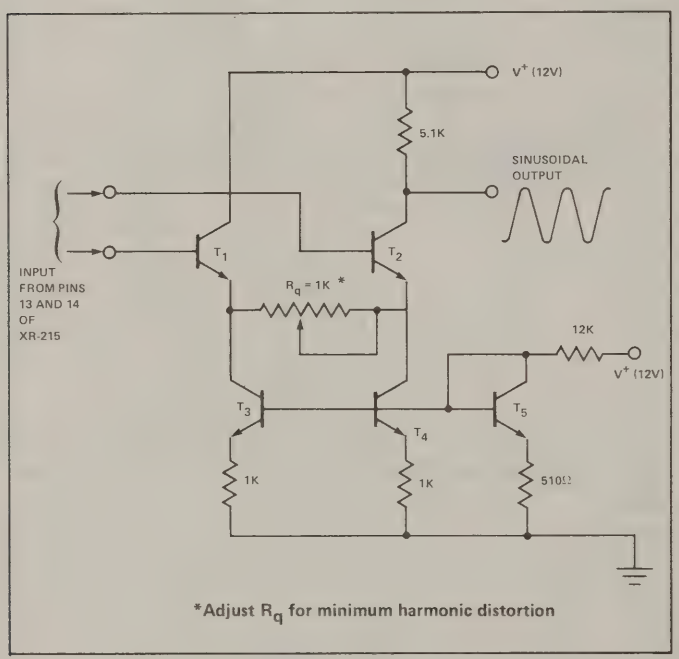


Figure 3. A Simple Triangle-to-Sinewave Converter Using a Differential Gain Stage

The sine-shaper circuit of Figure 3 can be designed by using the XR-C101 NPN transistor array, which provides five identical NPN transistors in a single IC package. Figure 4 shows the

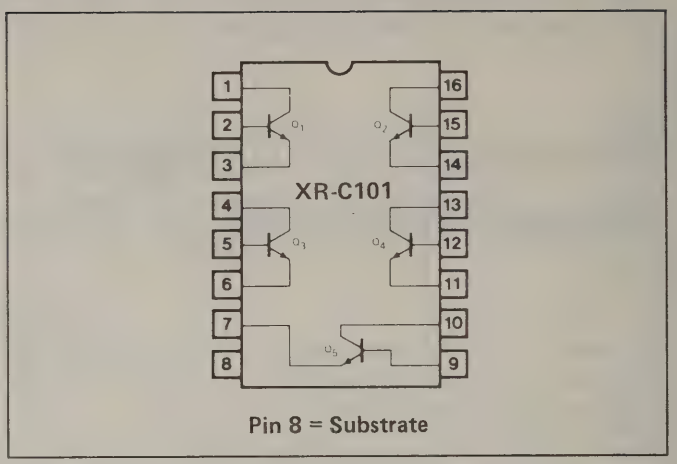


Figure 4. Package Diagram for XR-C101 Matched NPN Transistor Array

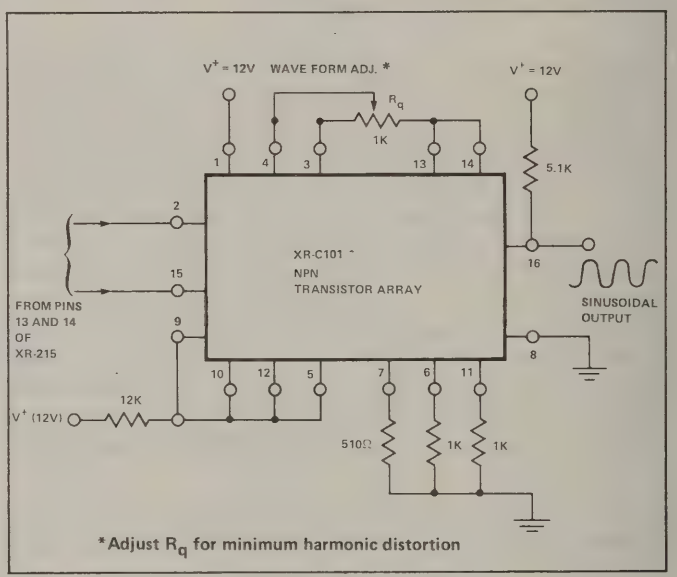


Figure 5. Use of XR-C101 Transistor Array to Obtain Sinusoidal Output from XR-215 PLL

package diagram of XR-C101 chip, in terms of its 16-pin DIP package.

The five independent transistors contained in the XR-C101 transistor array can be interconnected, as shown in Figure 5, to form the differential sinewave-shaping circuit of Figure 3. The inputs of the sine-shaper can be directly connected to the timing capacitor terminals (pins 13 and 14) of the XR-215 PLL.

Application Note AN-10

XR-C262 High-Performance PCM Repeater IC

INTRODUCTION

The XR-C262 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of $-40^{\circ}C$ to $+85^{\circ}C$. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Built-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The XR-C-262 operates with a single 6.8-volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock-extractor section of XR-C-262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to "off" state automatically when there is no input signal present. Compared to conventional repeater designs using discrete components, the XR-C262 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

This application note outlines the basic design principles and the electrical characteristics of the XR-C262 monolithic repeater IC. In addition, circuit connections and applications information are provided for its utilization in T-1 type 1.544 Megabit PCM repeater systems.

FUNDAMENTALS OF PCM REPEATERS

The Pulse-Code Modulation (PCM) telephone systems are designed to provide a transmission capability for multiple-channel two-way voice frequency signals which are transmitted in a digital PCM format. In order to minimize error rates, and provide transmission over long distances, this digital signal must be regenerated at periodic intervals, using a regenerative repeater system. Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator.

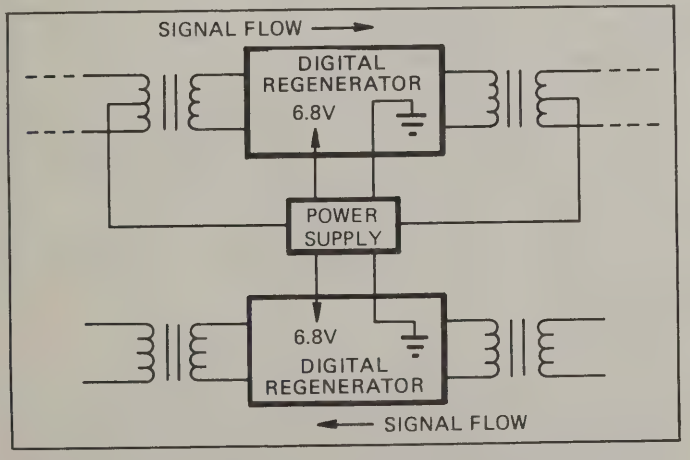


Figure 1. Block Diagram of a Bi-Directional Repeater System.

In the United States, the most widely used PCM telephone system is the T-1 type system which operates at a data rate of 1.544 Mbps, with bipolar data pulses. It can operate on either pulp- or polyethylene-insulated paired cable that is either pole-mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772 kHz is less than 36 dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The T-1 type transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end cross-talk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The XR-C262 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C262 ICs, one for each direction of information flow.

OPERATION OF THE XR-C262

The XR-C262 monolithic repeater is packaged in a 16-pin dual-in-line hermetic package, and is fabricated using bipolar process technology. The functions of the circuit terminals are defined in Figure 2, in terms of the monolithic IC package.

A more detailed system block diagram for the monolithic repeater system is given in Figure 3. The system blocks shown within the dotted area are included on the monolithic chip. The numbers on the circuit terminals correspond to the pin numbers of the 16-pin IC package containing the repeater chip. In terms of the system block diagram of Figure 3, the overall repeater operation can be briefly explained as follows.

The bipolar PCM signals which are attenuated and distorted due to the preceding transmission medium are applied to the input of a preamplifier (Block 1) through an Automatic Line Build-Out (ALBO) circuit. The impedance, Z_1, corresponds to the passive section of the ALBO network. The preamplifier section, along with the passive equalizer networks Z_2 and Z_3 connected in feedback around it, provides gain to compensate for line losses and band-limiting to reject unwanted noise as well as gain and phase equalization to shape received pulses.

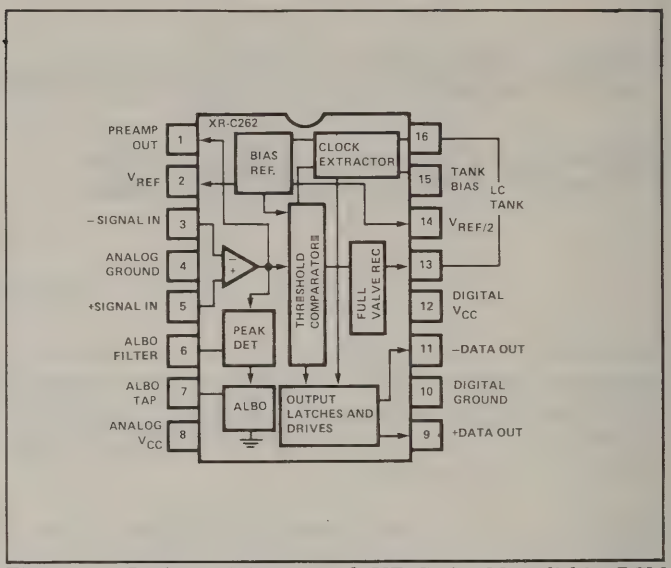


Figure 2. Package Diagram of XR-C262 Monolithic PCM Repeater.

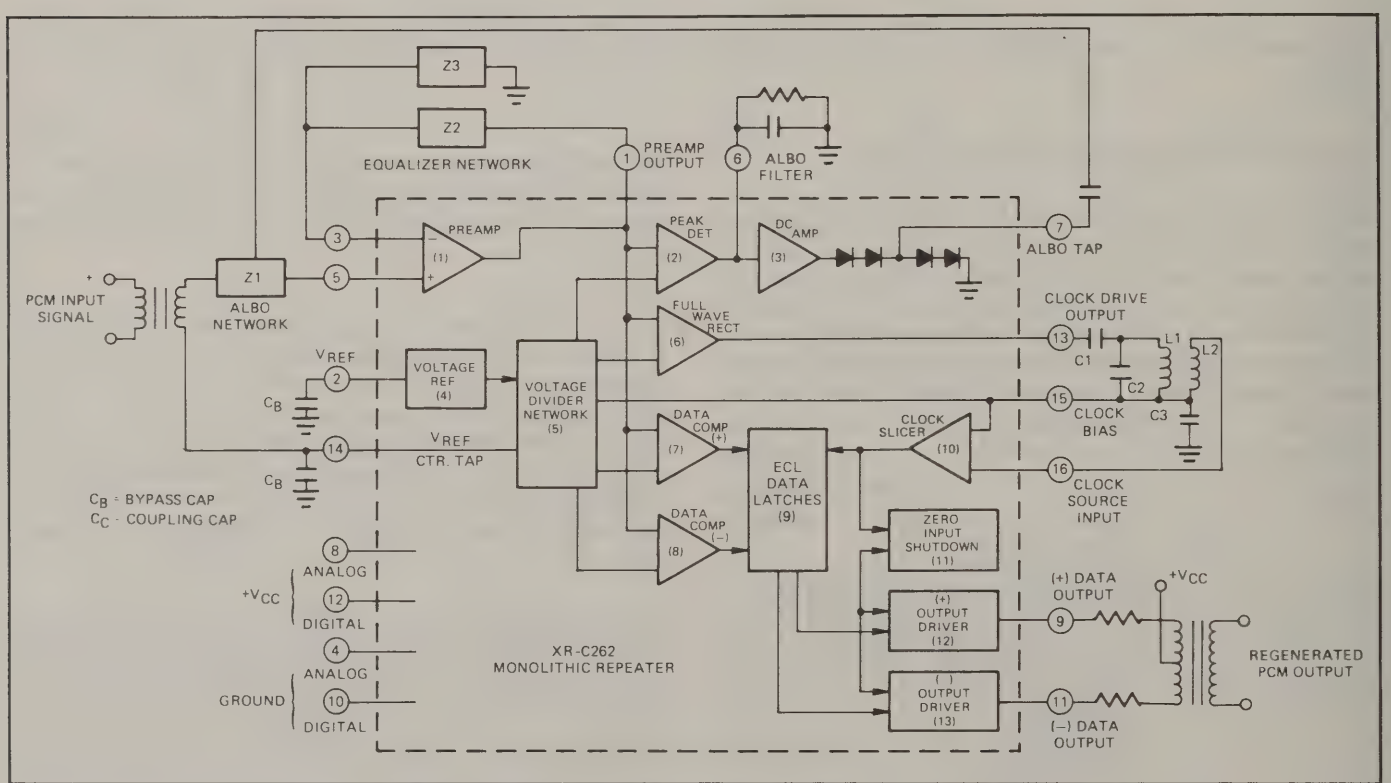


Figure 3. Detailed Block Diagram of the XR-C262 Monolithic Repeater System.

The ALBO circuitry provides attenuation and shaping to automatically adjust for varying cable characteristics. The output of the preamplifier is controlled to swing between two established peak levels. This is accomplished by feedback circuitry, and is similar in concept to automatic gain control. When the preamplifier output passes through the peak thresholds it is detected by the peak detector (Block 2) and produces a signal which is used to control a feedback loop establishing the attenuation and shaping of the ALBO network. The actual circuit design associated with this function is described in more detail in the discussion of peak detection and ALBO circuitry.

The output of the preamplifier drives a set of data comparators which are internally biased from a voltage reference (Block 4) and the precision voltage divider network (Block 5). Thus, the preamplifier output is "sliced" at various voltage levels to eliminate the effects of the baseline noise. This output is full-wave rectified and amplified through Block 6 of Figure 3. The resulting signal has a strong Fourier component at the clock frequency and is used to drive a high Q ($\approx$100) resonant circuit tuned to that frequency. The output of the resonant circuit is transformer-coupled to a zero-crossing detector and clock limiter (Block 10). The resultant output is the desired recovered timing. This resonant circuit is driven by a low impedance amplifier, and the resulting clock edges are in phase with the peak of the received pulses.

The regeneration of the data is achieved through the two data comparators (Blocks 7 and 8) and the ECL latches (Block 9) which function as tracking flip-flops. The positive and negative data paths are separate; and, with the exception of the data limiter and slicer levels, identical in design. The preamplifier output is sliced at about 45 percent of the peak voltage and its amplitude is limited to provide digital data pulses. The data is applied to one of the inputs to the tracking flip-flop, whose state is latched and unlatched by the clock. During acquisition, the flip-flop acquires data; during hold, further data transitions are ignored and the state of the flip-flop output determines whether an output pulse is transmitted. The implication of using the clock to perform data sampling is that path delays of the data and clock must be controlled to be equal. The monolithic integrated circuit technology affords this control. The advantage of this technique is that the need for clock shifting or strobe pulse generating circuitry for accurate sampling alignment is eliminated. Actual circuit implementation resulted in a 40 nsec misalignment of clock and data. This 40-nsec error in sampling time amounts to less than .4 dB degradation in SNR performance. Figure 4 shows the idealized timing and signal waveforms within the circuit.

The output drivers use latched data and clock to produce an output pulse-width which is accurately controlled by the duration of the clock. Non-saturating output drivers (Blocks 12 and 13) insure that output pulse rise and fall times are less than 100 nsec. The zero input shut-down circuitry (Block 11) guarantees that in the event incoming data disappears, the output switches will not latch in the "on" state. When no input signal is present, the absence of clock is sensed and the output drivers are held in the "off" state.

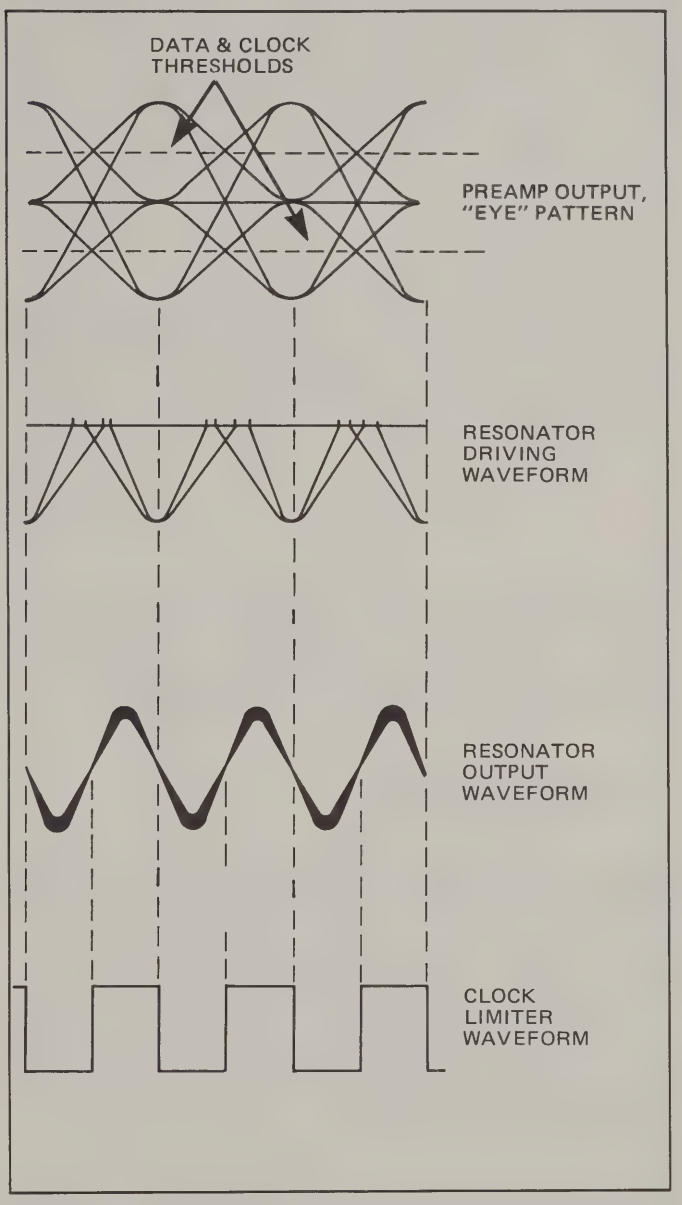


Figure 4. Timing Diagrams of Voltage Waveforms within the Clock Regeneration Section.

Figure 5 shows a practical circuit connection for the XR-C262 in an actual PCM repeater application for 1.544 Mbps T-1 repeater system. For simplification purposes, the lightening protection circuitry and the second repeater section for the reverse channel are not shown in the figure.

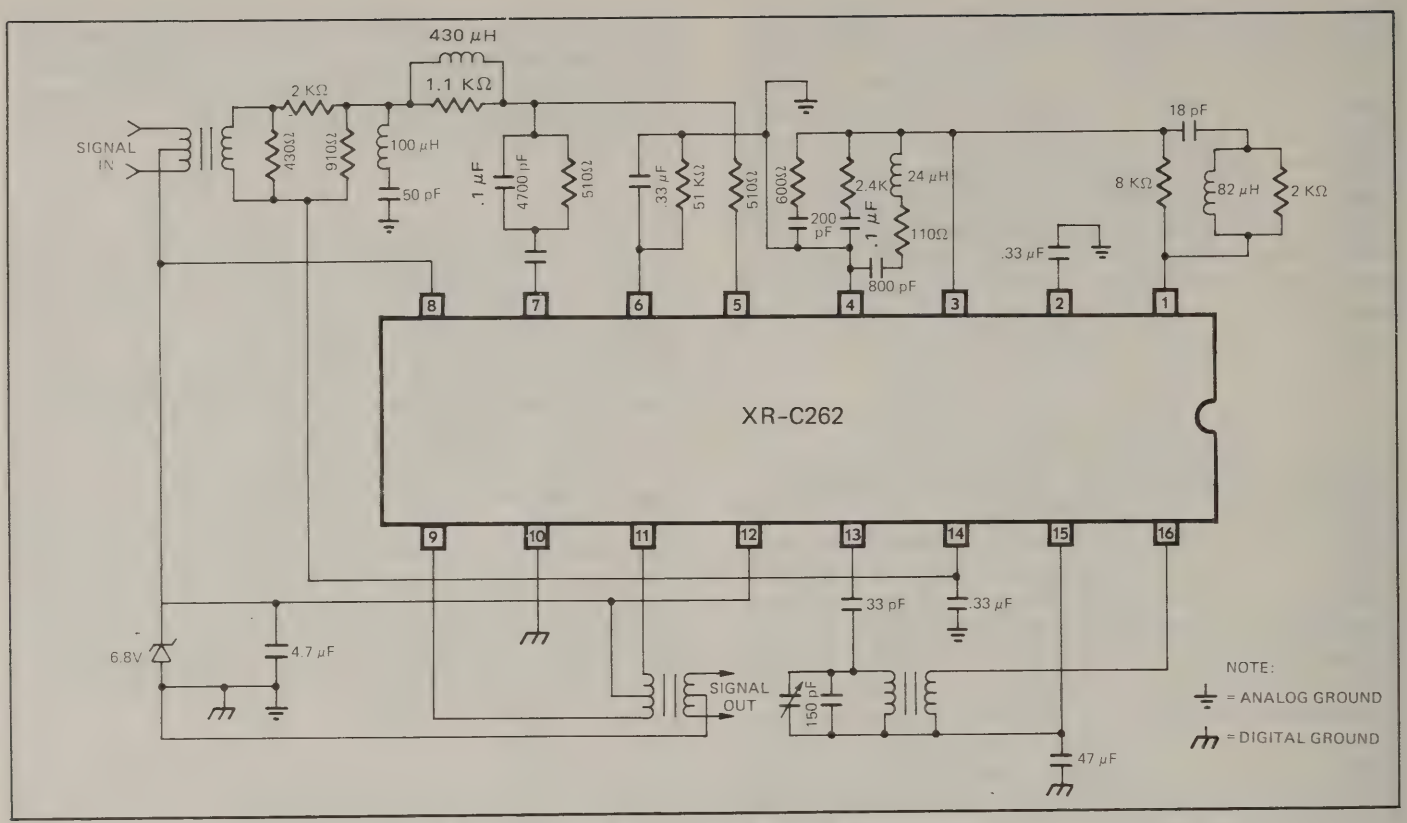


Figure 5. A Recommended Circuit Connection Diagram for T-1 Type Repeater Application.

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Figure 6):

The circuit diagram of the preamplifier section is shown in Figure 6. This section is designed as a single-stage high-gain amplifier with differential inputs and a single-ended output. The amplifier output is internally connected to the peak-detector, full-wave rectifier and the data-comparator sections. The circuit exhibits a high differential input resistance ($\approx 10^6$ ohms) and a low output impedance (≈ 80 ohms). It has a nominal voltage gain of 69 dB at DC and ≥ 50 dB at 1 MHz. The frequency response of the circuit exhibits a single-pole roll-off characteristics.

Peak-Detector and ALBO Section (Figure 7):

The peak-detector circuit is designed to detect the peaks of the preamplifier output, provided that these peaks exceed the internal detection threshold levels. This peak information is then low-pass filtered and is used to control the current in a diode string which acts as a variable-loss or "variolosser" element in a feedback path. In the circuit, the comparators conduct whenever the preamp output exceeds the (+) threshold in a positive direction or the (–) threshold in a negative direction. Transistor Q_5 then injects a pulse of current into the ALBO filter. In the steady state, DC level across the ALBO filter controls the current through the diode string; and the dynamic resistance of the diodes acts as the variolosser element. The usable linear resistance range in this application is almost three orders of magnitude ranging from 11Ω to ≈ 6 KΩ.

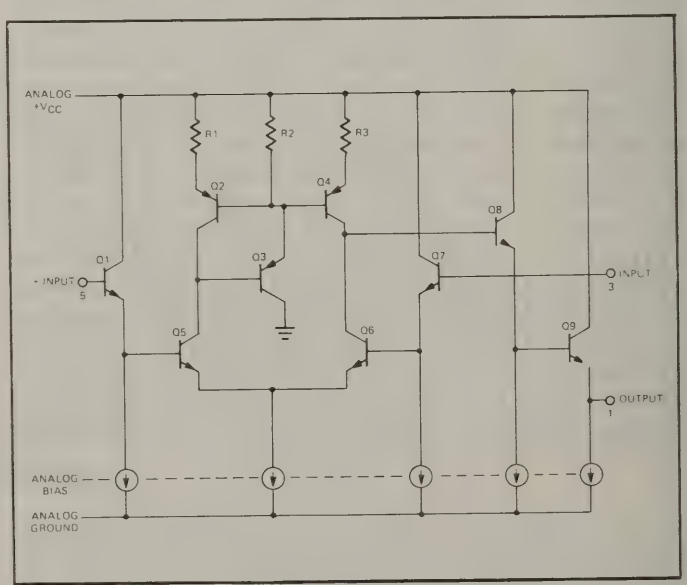


Figure 6. Circuit Diagram of Preamplifier Section.

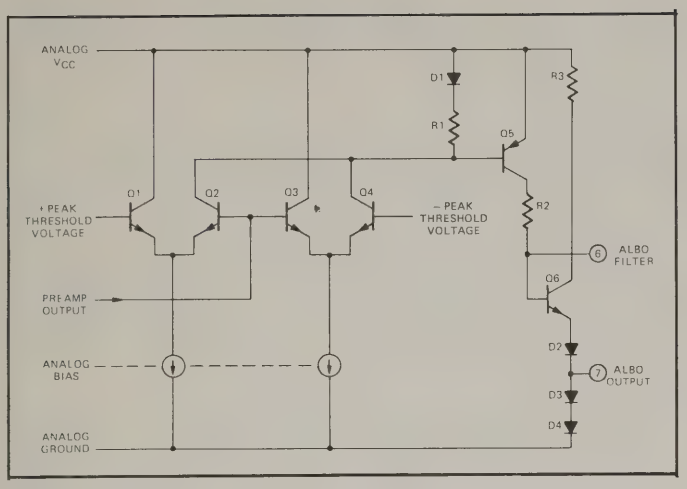


Figure 7. Circuit Diagram of the Peak-Detector and the ALBO Sections.

Data Latches (Figure 8):

The data latches are required to be impervious to data transitions in the latch mode, and to be "transparent," (i.e., tracking the input data) during the tracking mode. Figure 8 shows the basic circuit configuration used in the XR-C262, which meets the above-mentioned performance requirements. During the time when the clock pulse is high, the acquisition transistors Q_1 and Q_2 are differentially switched with data transitions, and the data is coupled to the respective bases of Q_3 and Q_4. When the clock pulse goes low at the sample time (see Figure 4), the information is regeneratively latched into Q_3 and Q_4. While the clock is low, further data transitions have no effect upon the state of the flip-flop. A more detailed description of the timing waveforms is given in Figure 13.

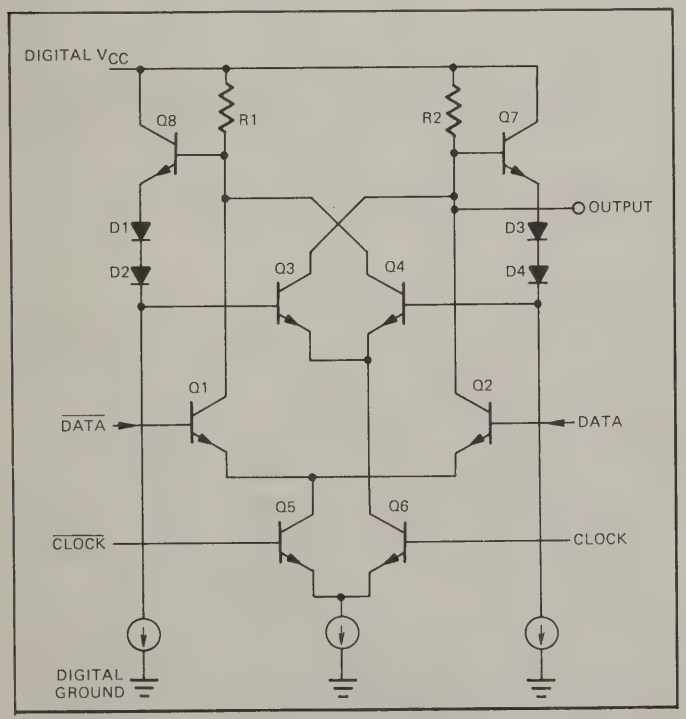


Figure 8. Circuit Configuration for Tracking Data Latches.

Threshold Circuitry (Figure 9):

Threshold circuitry is a low impedance voltage-divider circuit corresponding to Block 5 of Figure 3, and it establishes the fixed levels required for data, clock and peak detection. It is important that the thresholds are insensitive to temperature variations, and that they are of sufficiently low impedance to guarantee that there is no threshold variation due to changing signal conditions. The reference voltages of the peak-detector, data, and clock thresholds are set by a resistor chain which divides down the voltage of the on-chip zener diode. The ratios of data threshold to peak-detector threshold and that of clock threshold to peak-detector threshold are both set at 45 percent. In the actual circuit implementation, as shown in Figure 10, a compound connection of PNP's and NPN's are used to reduce the output impedance of the reference levels. The currents through the NPN and PNP transistor strings are set so as to insure that the base emitter voltage drops of the NPN's and PNP's are nominally the same. The output impedance of the resulting reference voltage taps are about 300 ohms. The center tap of the buffered divider is brought to a separate package terminal (Pin 14 of Figure 3) for biasing the preamplifier input.

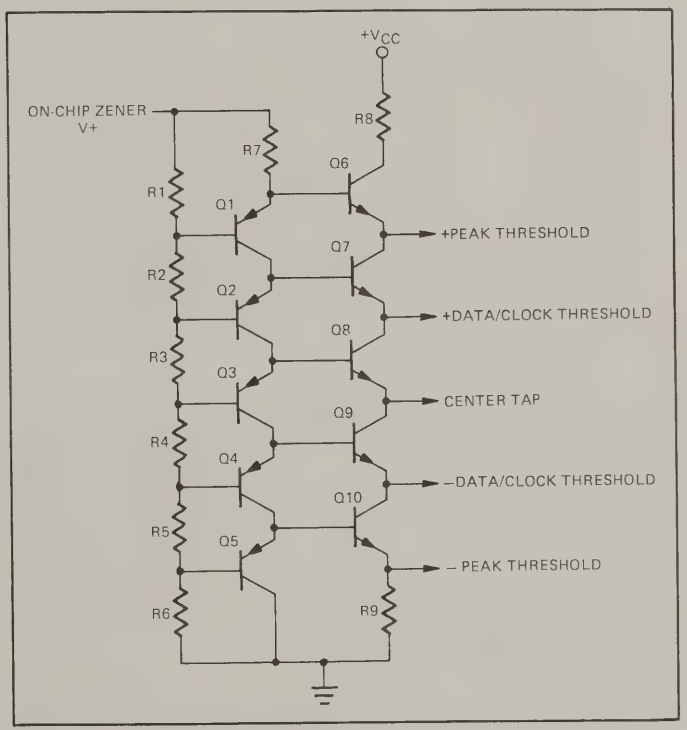


Figure 9. Internal Voltage-Divider Network for Comparator Threshold Setting.

Clock Recovery Section (Figure 10):

Clock recovery circuitry consists of a full-wave rectifier, an external L-C resonant circuit, a zero crossing detector, and limiting amplifier, as shown in Figure 10. The full-wave rectifier circuit, comprising of cross-coupled transistor pairs Q_1 through Q_4 has a net voltage gain of 2, which is obtained by Setting $R_1 = R_2 = (1/2)R_3$. The rectified output is then buffered by the Darlington emitter-follower stage made up of Q_5 and Q_6, and applied to the external L-C resonant circuit.

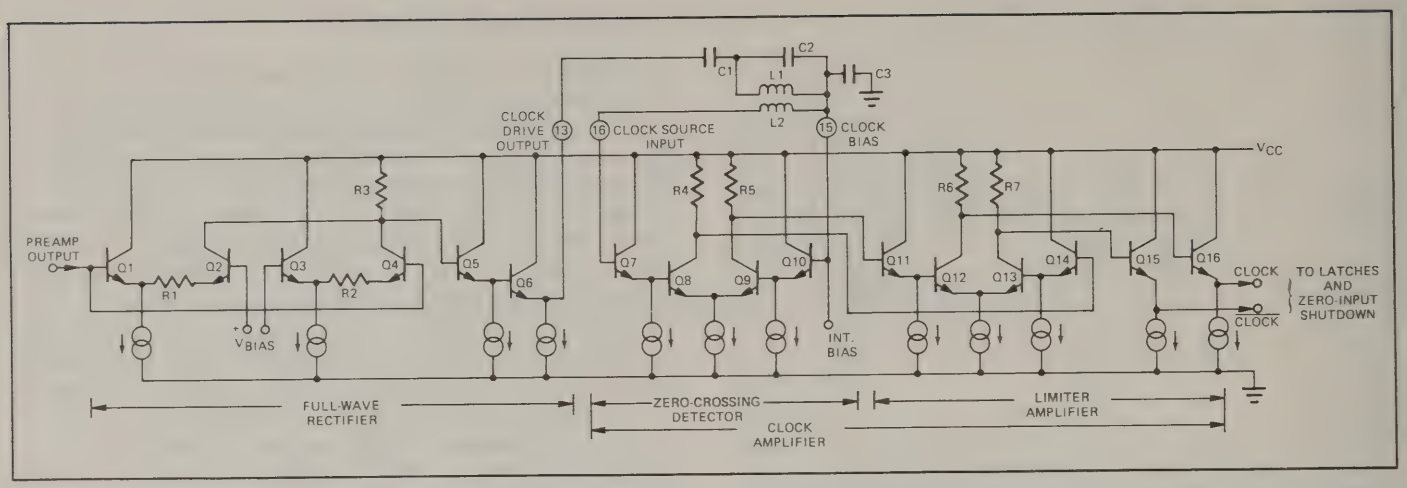


Figure 10. Circuit Diagram of the Clock Recovery Section.

Q_6 is operated at a high bias current level to provide an output impedance of less than 15Ω. This low impedance is required to insure that the L-C tank-drive circuitry looks like a voltage source.

The inductor of the resonant tank circuit is also a transformer which couples the sine wave signal to the zero crossing detector and limiting amplifier. The zero crossing detector is a differential amplifier with a nominal voltage gain of 20 and input impedance of 4 MΩ. The sine wave from the resonant circuit is sliced to produce a square wave with sharp transitions at the zero crossings. This eliminates timing variations that may be caused by amplitude changes of the sine wave signal. The output of the zero crossing detector is further enhanced by the limiter which is another differential pair with a nominal voltage gain of 30. The output of this amplifier is a 1.5V peak-to-peak square wave clock which drives the data latches and the output drivers.

Zero-Input Protection Circuit (Figure 11):

The zero input protection circuitry accomplishes the dual task of preventing the output switches from latching in an "on" state, as well as reducing the likelihood of output pulses with no input signal. The data, clock, and regenerator circuitry are all balanced DC coupled circuits. Controlling the steady state, no-signal condition of these circuits without building an unacceptable offset into the path is not practical. Instead, a retriggerable one-shot that uses the saturation characteristics of PNP transistors is used to control the level of the clock into the output switches. This technique uses the bandpass characteristics of the timing recovery resonant circuit to reject out of band signals thus minimizing the chance of producing output pulses with no input signal and the presence of noise. Figure 11 shows the basic implementation of the zero-input protection circuit. Q_1 and Q_2 function as a simple retriggerable one-shot. The transistor Q_2 is a lateral PNP device with a limited frequency capability and long storage-time delay. The existence of the 1.544 MHz clock causes Q_2 to saturate and remain in saturation while clock pulses are present. The comparatively long time constant associated with Q_2 coming out of saturation ($\approx$ 5 μsec) insures that, when data is present, the zero input protection has no effect upon operation. When data disappears there is no clock to retrigger the one-shot, thus Q_2 comes out of saturation, causing Q_3 to saturate which pulls the respective clock lines high, and disables both output drivers in their "off" state.

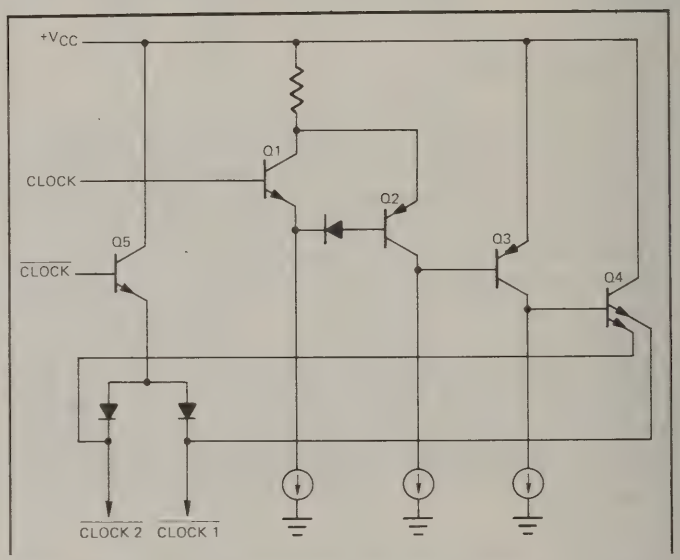


Figure 11. Zero-Input Shutdown Circuit for Output Protection.

Output Drive Circuitry (Figure 12):

The output drive circuitry is made up of two identical channels as indicated in the block diagram of Figure 2. The circuit configuration for each of these driver sections is shown in Figure 12. The output would follow the data input from the latches only when the clock input is at a "high" state, i.e., with Q_2 off and Q_3 on. In this manner, the output pulse-width is controlled by the clock. To provide the fast turn-on and turn-off of the output drivers, all the transistors operate in a nonsaturating state. Q_4 forms an active clamp to reduce voltage swing at the base of Q_6, and the clamp diode D_5 prevents the saturation of the output driver Q_7. Because of the biasing scheme mentioned above, the amplitude of the clock and the latched data are insensitive to supply voltage and temperature changes. Thus, the variations of the regenerated pulse-width over temperature and supply are minimized.

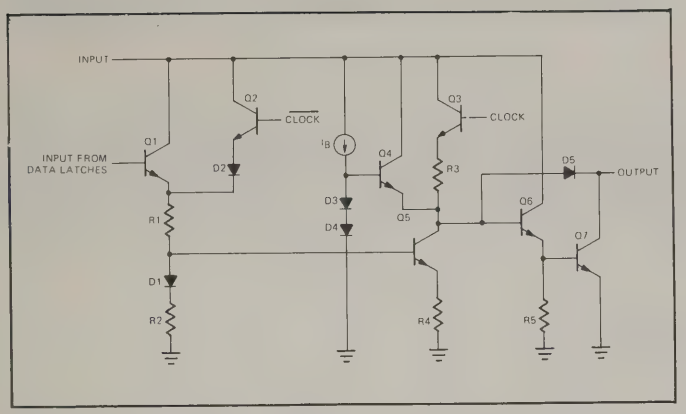


Figure 12. Circuit Configuration for the Output Drivers.

Timing Waveforms (Figure 13):

Figure 13 illustrates the relative time and phase relationships between the signal levels at various points within the circuit. For the purpose of illustration an input data pattern comprised of a string of "ONE"s is assumed, which looks like a nearly sinusoidal input, after having traveled through a dispersive transmission medium such as a long cable. Waveform (1) is the output of the preamplifier; waveforms (2) through (5) are the outputs of the two data comparators driven by the preamplifier output (see Figure 3). Waveform (6) is the low-level clock signal obtained from the resonant tank circuit, at pin 16 which is then amplified and "sliced" by the clock-recovery circuitry (see Figure 11) and appear as the internal clock signals shown as waveforms (7) and (8). The waveform (9) shows the output of one of the data latches (Figure 8) as a function of the clock and data inputs. The output of the latch tracks $\overline{+DATA}$ when the clock is low, and stays latched in that condition when the clock goes high. The output drive at pin 9, which is shown as waveform (10) will then go low only when the waveforms (8) and (9) are low. The waveform (11) shows the second output available at pin 11. These two outputs are then differentailly combined by the output transformer (see Figure 3) to provide the regenerated bipolar output pulses shown in waveform (12) of Figure 13.

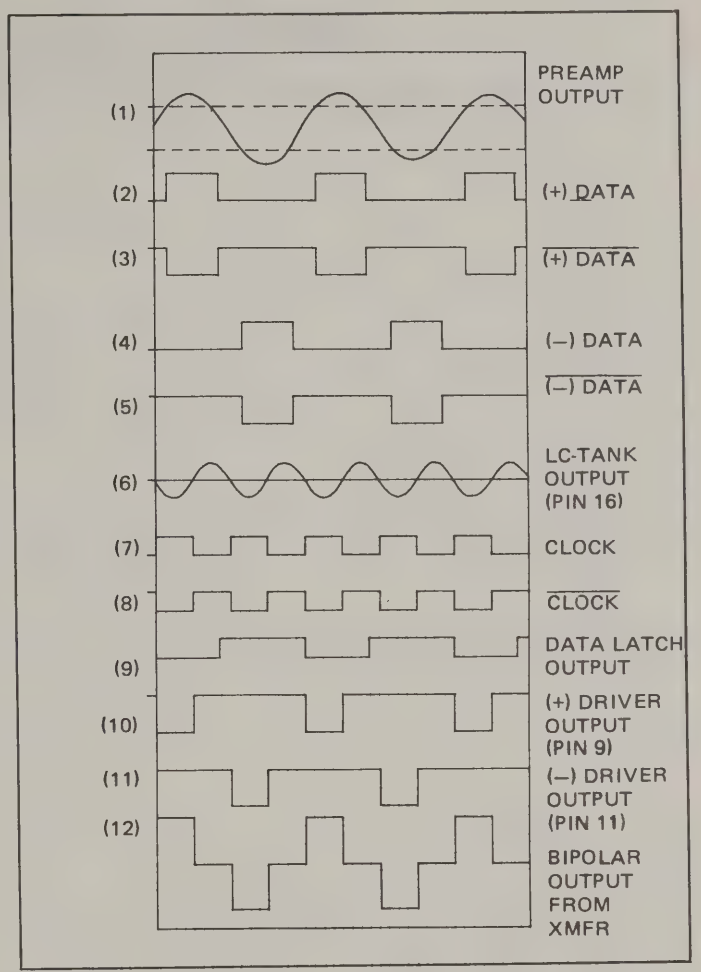


Figure 13. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern.

ELECTRICAL CHARACTERISTICS

$+V_{CC}$ = 6.8 Volts, T_A = –40°C to +85°C.

CHARACTERISTICS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	–15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
Comparator Thresholds					Measured at Pin 1 relative to Pin 14
ALBO Threshold	0.75	0.9	1.1	V	
Clock Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					Measured at Pins 9 and 11
Output High Swing	5.9	6.8		V	R_L = 400Ω
Output Low Swing	0.6	0.7	0.9	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	294	324	354	nsec	
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

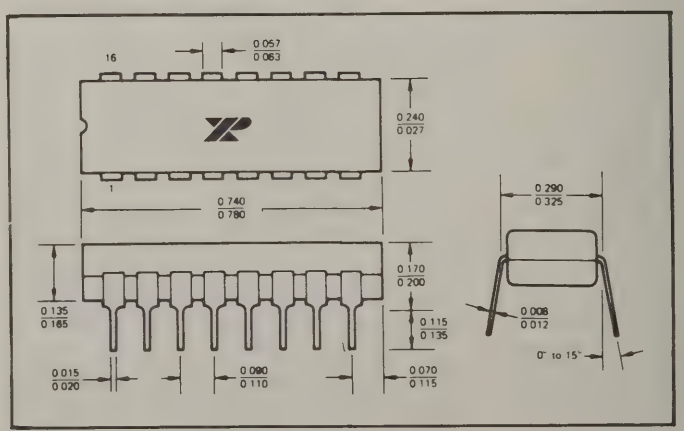
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Storage Temperature Range	–65°C to +150°C

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-C262	CERDIP	–40°C to +85°C

PACKAGE INFORMATION



Application Note AN-11

A Universal Sine Wave Converter Using the XR-2208 and the XR-2211

INTRODUCTION

A universal sine wave converter is a system block which can convert *any* periodic input signal waveform to a low-distortion sine wave, whose frequency is identical to the repetition rate of the periodic input signal. Such universal sine wave converters find applications in communications and telemetry systems. They are particularly useful for converting transducer output waveforms, or pulses, into clean sine wave signals over a band of frequencies. This conversion to sine wave is often necessary to reduce the required system bandwidth for signal transmission by eliminating the harmonic frequencies of the signal.

In the cases where the input frequency is known, and does not change, the universal sine wave converter can be replaced by a simple high-Q filter, tuned to the input frequency. However, in many cases the input frequency, or the repetition rate, is *not* constant, but varies as a function of time or input data. In such cases a fixed-frequency filter is not feasible, and one is forced to use a universal sine wave converter which is esentially a *"tracking regenerative filter"*.

In this application note, the design principle and the performance characteristics of a regenerative sine wave converter circuit is described. The circuit operates on the phase-locked loop (PLL) principle and can be implemented using the XR-2211 monolithic PLL tone decoder and the XR-2208 multiplier IC.

PRINCIPLE OF OPERATION

Figure 1 shows the functional block diagram of a regenerative sine wave converter system, comprised of four functional blocks: (1) a phase-locked loop (PLL), (2) a sine-shaper, (3) a keyed amplifier, and (4) a lock-detect circuit. With reference to the figure, the principle of operation of the entire system can be briefly explained as follows:

When a periodic input signal is present at the input, within the tracking range of the PLL, the circuit would "lock" to the input signal; and the output of the voltage-controlled oscillator (VCO) section of the PLL will duplicate the frequency of the input signal. However, the VCO output waveform will have a fixed wave shape (normally a triangle wave) independent of the input waveform or amplitude. The output of the oscillator section then can be connected to a triangle-to-sine wave converter which converts it to a low-distortion sine wave. The output of the triangle-to-sine converter is then applied to a variable-gain amplifier which sets the desired output amplitude. Since the oscillator section of the PLL is always running, the circuit also contains a "lock-detect" section which *enables* the output amplifier only when there is an input signal. Thus, with no input signal present within the bandwidth of the PLL, the lock-detect section will keep the output amplifier in the "off" state, and the circuit will not produce an output signal.

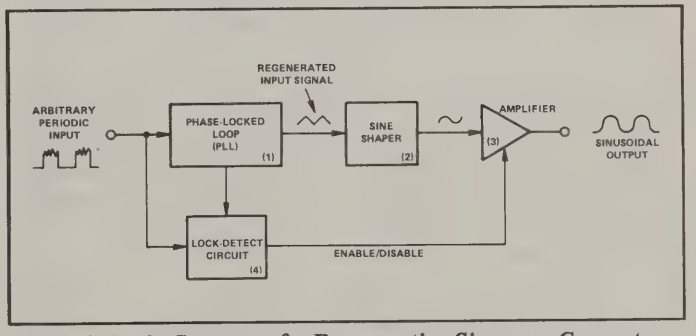


Figure 1. Basic Concept of a Regenerative Sinewave Converter.

CIRCUIT DESIGN

The basic regenerative sine wave converter system of Figure 1 can be easily implemented using the XR-2211 monolithic tone decoder and the XR-2208 monolithic multiplier IC's, with only a minimum number of external components.

The XR-2211 is a monolithic PLL circuit especially designed for FSK and tone detection. Thus, it contains the complete PLL and lock-detect sections (Blocks 1 and 4 of Figure 1) on the same chip. Its overall block diagram is shown in Figure 2. The circuit is packaged in a 14-pin dual-in-line package; and the functions of the circuit terminals are given in Figure 3 in terms of the monolithic IC package. In the sine wave converter

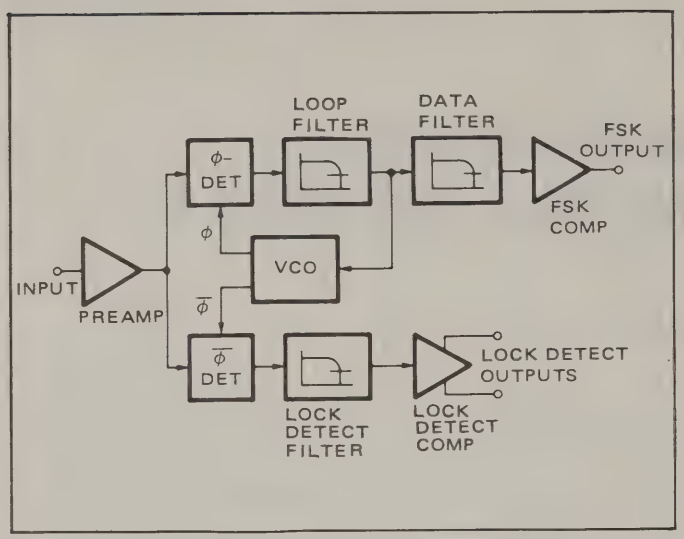


Figure 2. Block Diagram of XR-2211 Phase-Locked Loop FSK and Tone Decoder IC.

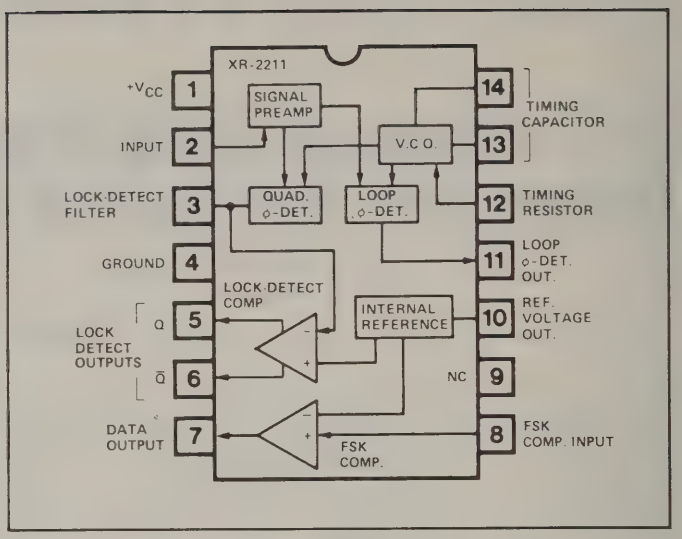


Figure 3. Package Diagram of XR-2211 PLL Circuit.

application, the FSK detector portion of the circuit is not used; only the basic phase-locked loop and the lock-detector sections are utilized. Figure 4 illustrates the necessary external components for its application in the sine wave converter system. The oscillator section of the XR-2211 is an emitter – coupled multivibrator which oscillates by charging and discharging the external timing capacitor, C_O, (connected across pins 13 and 14) through internal constant-current stages. Thus, the output waveform, taken differentially across the timing capacitor, is a linear triangle wave. This waveform can then be converted to a low-distortion sine wave by the XR-2208 multiplier.

The XR-2208 is a monolithic multiplier circuit which contains a four-quadrant analog multiplier, an op amp, and a unity-gain buffer amplifier in a 16-pin dual-in-line package. Its functional block diagram and equivalent circuit schematic are given in Figures 5 and 6, respectively.

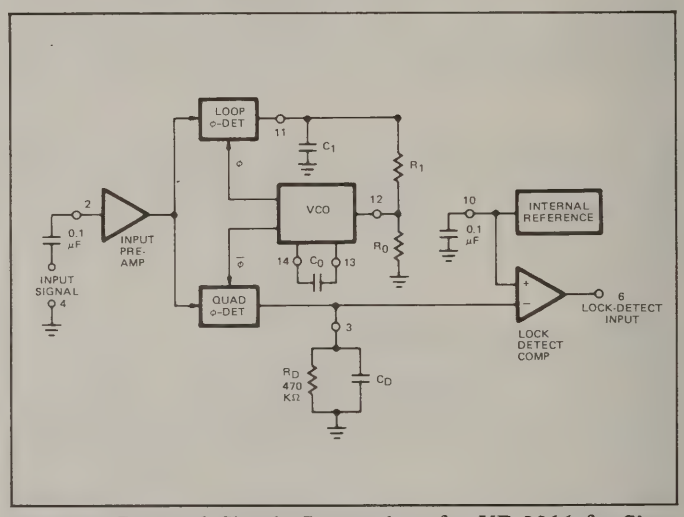


Figure 4. External Circuit Connections for XR-2211 for Sine-wave Converter Application.

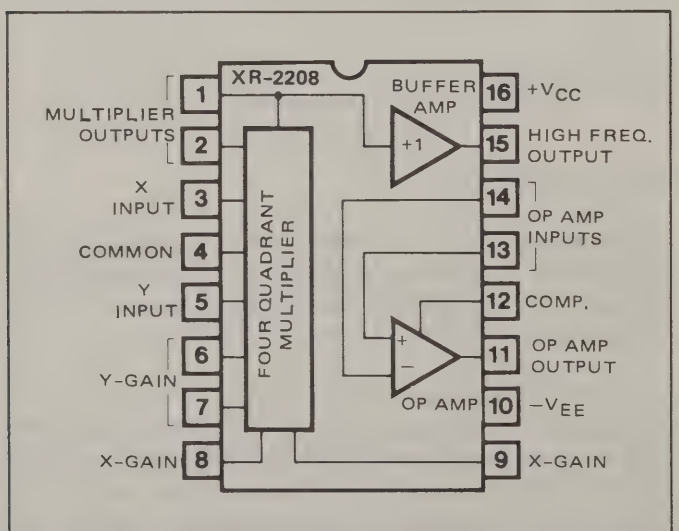


Figure 5. Block Diagram of XR-2208 Operational Multiplier.

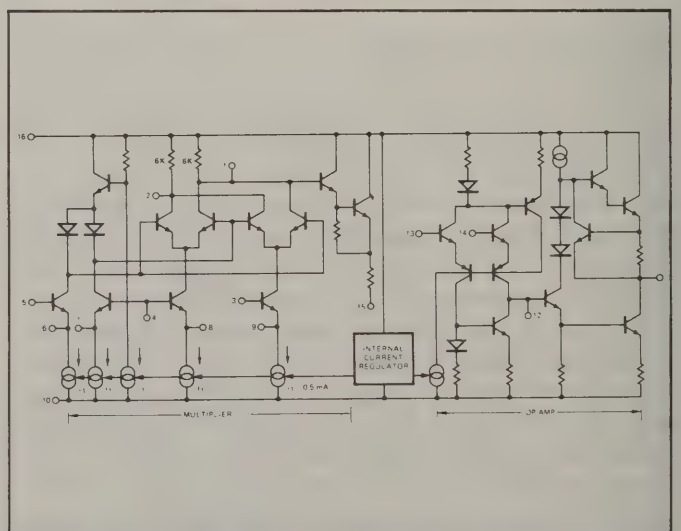


Figure 6. Simplified Circuit Schematic of the XR-2208 Operational Multiplier.

Figure 7 shows the recommended circuit connection of the XR-2211 and the XR-2208 to form a universal sine wave converter circuit. In the figure, a non-crital zener diode ($V_Z \approx$ 6V to 7V) is used to reduce the supply voltage applied to XR-2211, to facilitate DC coupling between the two chips. The frequency of the VCO section of the XR-2211 is set by the timing components R_O and C_O. In this application, a fixed value of R_O = 10KΩ is recommended, giving a center frequency, f_O value of:

$$f_o = \frac{100}{C_o(\mu F)} \text{ Hz}$$

The triangle wave oscillator output of the XR-2211 PLL is attenuated through a resistive divider made up of two 10KΩ resistors, and a variable 10KΩ potentiameter, R_X. The attenuated triangle wave across R_X is then applied differentially to the X-input (pins 4 and 5) of the XR-2208. The 100Ω external resistor across Y-gain setting terminals (pins 6 and 7) causes the Y-input of the multiplier to be slightly overdriven, and thus causes the peaks of the triangle input rounded into a low-distortion sine wave.

The distortion of the sine wave is minimized by adjusting R_X, which sets the triangle wave amplitude. The sinusoidal output is available at the unity-gain buffer terminal (pin 15) of the XR-2208. This output is then level-shifted toward ground, through two 10KΩ resistors, and is AC coupled to the inverting input of the op amp section of XR-2208. The gain of the op amp is externally adjusted by means of the 500KΩ potentiometer, R_F. The DC voltage level of the op amp output is set at the reduced supply voltage (i.e., V_{CC} -V_Z).

The lock-detect output of the XR-2211 (pin 6) is shorted to the mid-point of the resistive divider at pin 15 of the XR-2208. With no input signal present at the input within the lock range of the XR-2211, pin 6 is at a "low" state. Thus it acts as a shorting switch to ground and disables the op amp section of the XR-2208. When a periodic input signal appears at the circuit input and the XR-2211 establishes lock with the signal; the lock-detect output at pin 6 goes to a "high" or non-conducting state and enables the output op amp of the XR-2208; and a low-distortion sine wave output is obtained at the output (pin 11 of XR-2208).

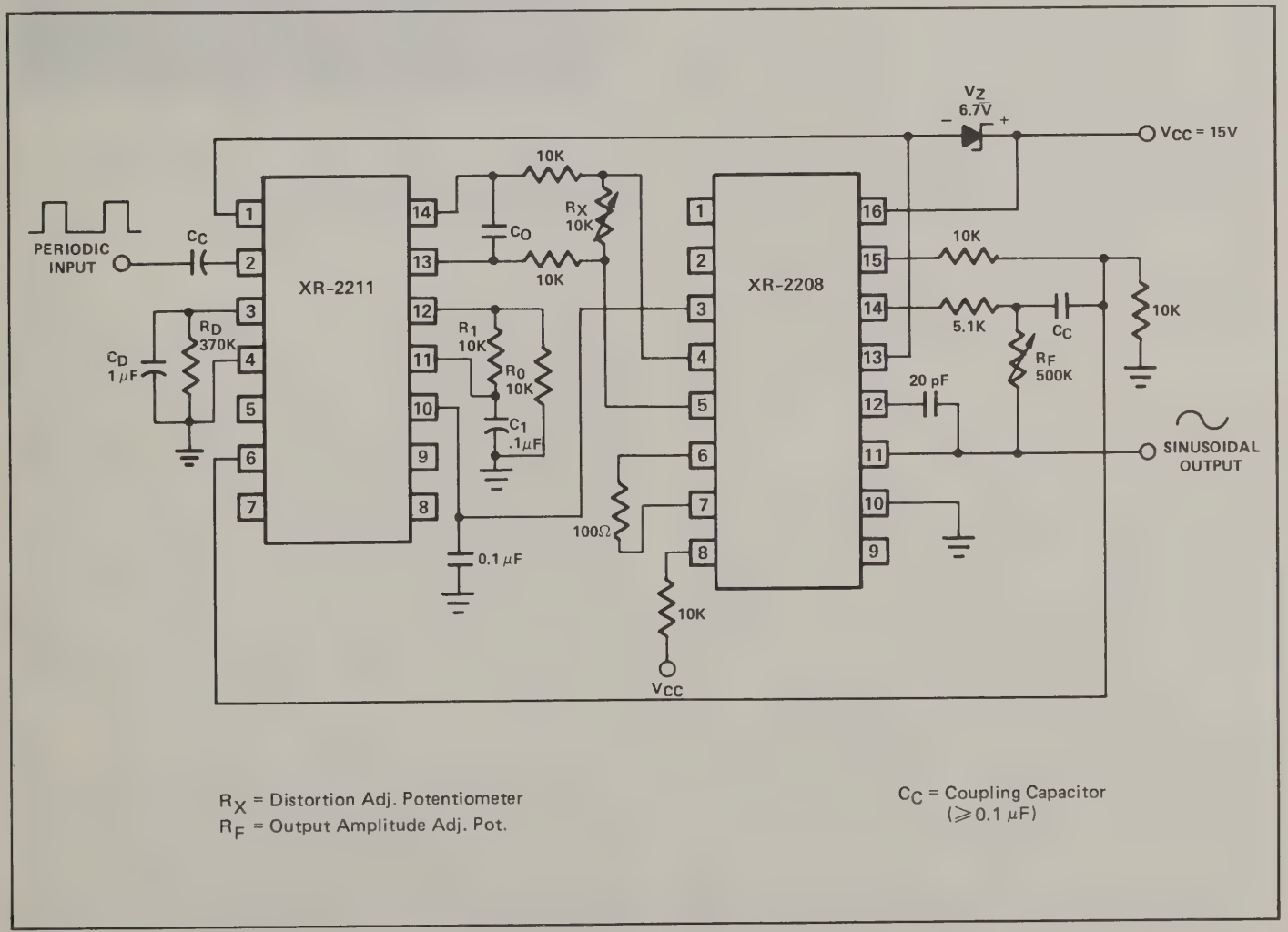


Figure 7. Recommended Circuit Connection for the Regenerative Sinewave Converter.

The circuit of Figure 7 can operate as a sine wave converter, over a frequency band between two frequencies f_H and f_L corresponding to the upper and lower lock ranges of the PLL. With the components shown in the figure, this corresponds to approximately ± 30% bandwidth around the center frequency, f_o, for inputs with close to 50% duty cycle. For periodic inputs with less than 50% duty cycle, this lock range is reduced further. For example, for inputs with 20% duty cycle, this bandwidth drops to about ± 10% of center frequency. The operation of the circuit with input signals having less than 10% (or more than 90%) duty cycle is not practical. The minimum input level required for circuit operation is 10mV rms. The circuit can generate a nearly sinusoidal output with input signals from very low frequencies up to 100 kHz. Typical distortion characteristics of the output are shown in Figure 8, as a function of frequency of operation. Figure 9 shows a typical example of input and output waveforms for the sine converter circuit of Figure 7, operating at 1 kHz input repetition rate, with a noisy input signal.

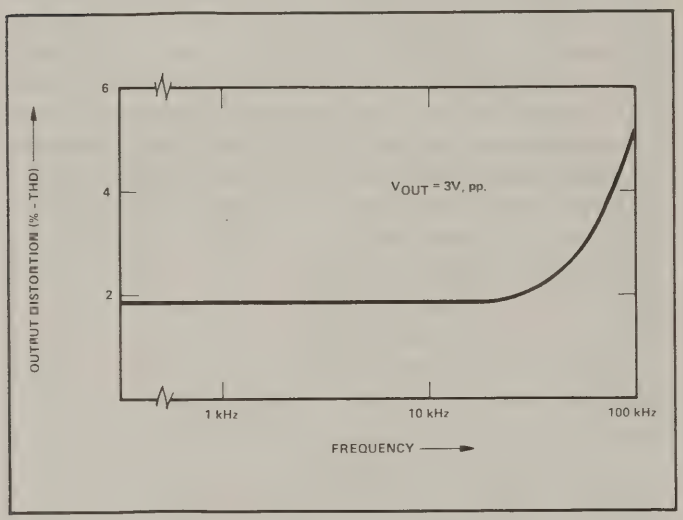


Figure 8. Output Distortion vs Frequency.

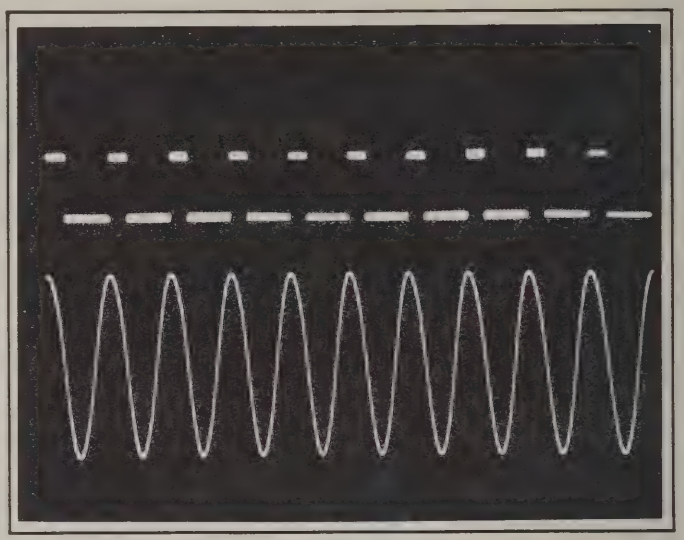


Figure 9. Typical Input-Output Waveforms.

(Top: Noisy Input Signal; Bottom: Sinusoidal Output.)
Scale: Vertical: 1 Volt/Div.
Horizontal: 1 m Sec./Div.

Application Note AN-12

Designing High Frequency Phase-Locked Loop Carrier-Detector Circuits

INTRODUCTION

The phase-locked loop (PLL) system can be converted to a frequency-selective tone- or carrier-detection system by the addition of a "quadrature detector" section to the basic PLL. Such a carrier-detect system serves as a "lock indicator" for the PLL and produces a logic signal at its output when there is a tone or a carrier signal present within the lock range of the phase-locked loop.

A number of monolithic tone-decoder IC's have been developed which implement the quadrature-detection technique for detection of low frequency tones, such as those used for telephone dialing or ultrasonic remote control. However, because of the particular PLL designs used in these monolithic detectors, their applications are limited to frequencies below 100 kHz. This application note describes a circuit approach, using the XR-210 or the XR-215 high frequency PLL's, along with the XR-2228 monolithic multiplier/detector, which extends phase-locked loop tone detection capabilities to frequencies up to 20 MHz.

PRINCIPLE OF OPERATION

The basic block diagram of a phase-locked loop tone detector system is shown in Figure 1. Such a detector system produces a logic-level signal at its output, when the PLL is locked on an input signal. It is made up of two main sections:

1. A PLL section which synchronizes or "locks" on the input signal.

2. A "quadrature detector" section made up of a phase-detector, a low-pass filter and a voltage-comparator.

Its principle of operation can be briefly described as follows: When the PLL is locked on an input signal, its voltage-controlled oscillator (VCO) section produces a set of input signals, Φ_1 and $\bar{\Phi}_1$, which are 90° apart in phase, but have the same frequency as the input signal to be detected. One of these signals, Φ_1, is used to drive the PLL phase detector; the other output, which is called the "quadrature output" is used to drive a "quadrature phase-detector", as shown in Figure 1. If the PLL is locked on the input signal, then the input signal and the VCO signal applied to the quadrature phase-detector are coherent in phase and frequency. This causes a DC level shift at the low-pass filtered output of the quadrature phase-detector and makes the voltage comparator output change its output logic state. Thus, an output logic signal is produced indicating the "lock" condition of the PLL.

This type of tone detection technique is a special case of the "synchronous AM detection" principle, discussed in detail in Exar's Application Note AN-13. The key difference between the tone detection and the synchronous AM detection application is that, in the case of the tone detection, a binary logic output is produced, corresponding to the "*presence*" or the "*absence*" of the desired input tone, rather than an analog demodulated signal.

XR-210 AND XR-215 HIGH FREQUENCY PLL CIRCUITS

The XR210 and the XR-215 are high frequency phase-locked loop detector and demodulator circuits. Their functional block diagrams are shown in Figures 2 and 3. Both circuits are packaged in 16-pin dual-in-line packages and contain high frequency VCO and phase-detector sections. The XR-215 chip also contains an operational amplifier. In the case of the XR-210, this op amp section is replaced by a high-gain voltage comparator which drives an open-collector type logic output. The XR-210 is particularly intended for FSK demodulation and can operate up to 20 MHz. The XR-215 is designed for linear FM detection and is suitable for frequencies up to 35 MHz. Except for the frequency capability of the VCO, the oscillator and the phase-comparator sections of both circuits are quite similar.

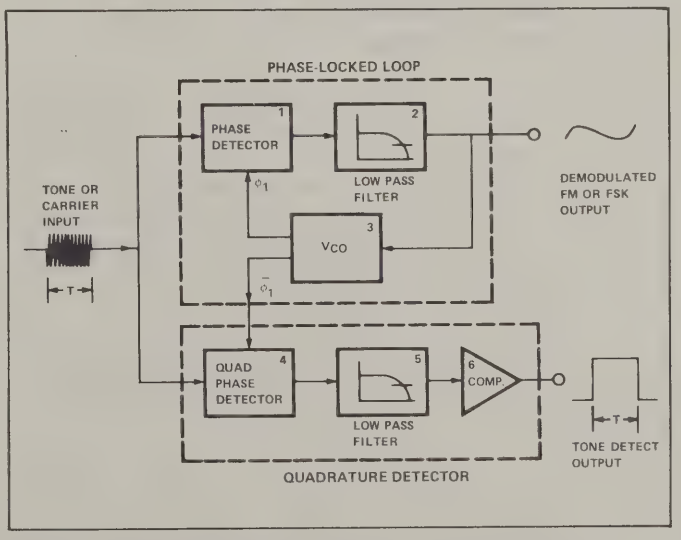


Figure 1. Functional Block Diagram of a PLL Tone- or Carrier-Detector System

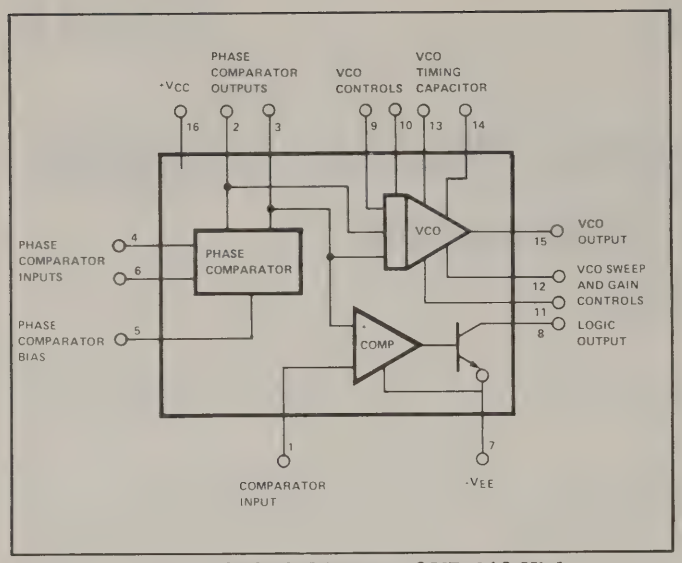


Figure 2. Functional Block Diagram of XR-210 High-Frequency FSK Modulator/Demodulator

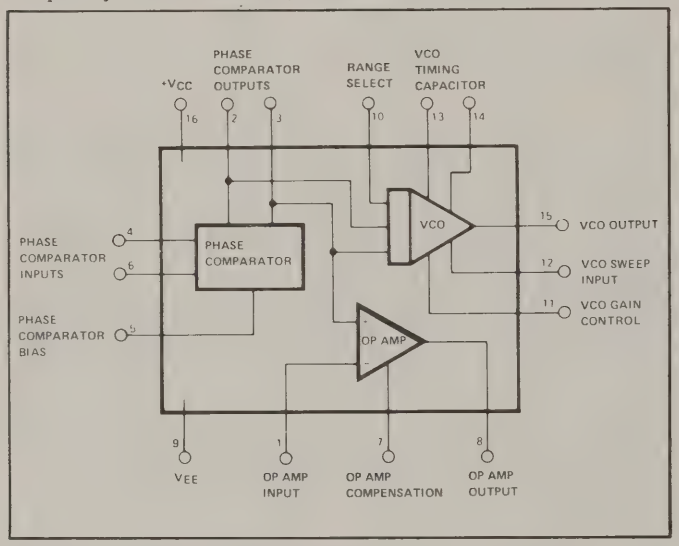


Figure 3. Functional Block Diagram of XR-215 High-Frequency Phase-Locked Loop

The VCO section of the XR-210 or the XR-215 does not provide a separate "quadrature output", which is 90° phase-shifted with respect to the basic VCO output (pin 15). However, the triangular output available across the VCO timing capacitor terminals (pins 13 and 14) can serve as such a quadrature output if it is amplified and "sliced" externally, as shown in the timing diagram of Figure 4.

XR-2228 MULTIPLIER/DETECTOR CIRCUIT

The XR-2228 is comprised of a four-quadrant multiplier and a high-gain op amp on a single monolithic chip. It is packaged in a 16-pin dual-in-line package and has the functional block diagram shown in Figure 5. It contains independent and fully differential X- and Y-inputs which makes it easy to interface with the XR-210 or the XR-215 type PLL circuit for carrier-detection applications. In the tone- or carrier-detect application, the multiplier section of the XR-2228 is used as the "quadrature phase-detector" section of the block diagram of Figure 1. The op amp is used as a high-gain voltage comparator which converts the differential voltage level changes at the multiplier outputs into logic level output signals.

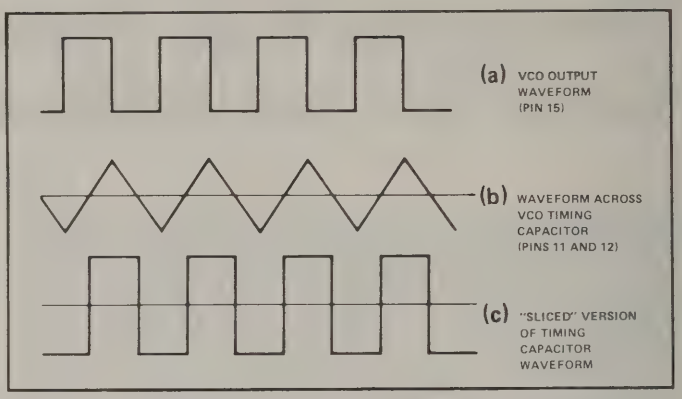


Figure 4. Timing Diagram of VCO Output Waveforms Available from XR-210 or XR-215 High-Frequency PLL Circuits

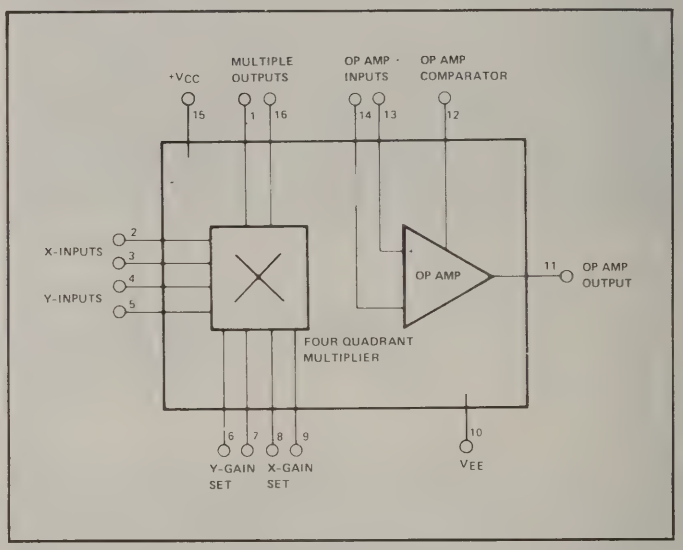


Figure 5. Functional Block Diagram of XR-2228 Multipler/Detector

CIRCUIT OPERATION

Figure 6 shows the generalized circuit connection of the XR-2228, along with either the XR-210 or the XR-215 high frequency PLL IC, for tone- or carrier-detection application. Since the external connections for the XR-210 or the XR-215 are the same as those given in their respective data sheets, only the external circuitry associated with the XR-2228 is shown in the figure. The circuit, as shown, can operate with a single power supply, from 10V to 20V, or with split supplies in the range of ±5V to ±10V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 6 to ground.

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used, and to the X-input terminal (pin 2) of the XR-2228.

The Y-inputs (pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at pins 13 and 14 of the PLL IC) which is AC coupled to pins 4 and 5 of the XR-2228 multiplier input. The multiplier input stage "slices" this signal to produce the quadrature frequency waveform shown in Figure 4(c).

The differential DC voltage level at the multiplier output terminals (pins 1 and 6) is offset by means of an external resistor, R_A, as shown in Figure 6. This initial offset causes the op amp output of the XR-2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 6, the op amp output (pin 11) would be at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (i.e., near $+V_{CC}$) when the PLL circuit is "locked" on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

The filter capacitor, C_A, connected across pins 1 and 16 of the multiplier outputs, serves as the post-detection low-pass filter (Block 5 of Figure 1). The time constant of this filter is equal to (C_A R_B) where R_B ($\approx 8k\Omega$) is the internal resistance of the IC at pins 1 and 16. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

The detection threshold (i.e., minimum detectable input signal amplitude) varies inversely with the multiplier gain-setting resistor R_X. Figure 7 shows the typical detectable signal level, as a function of R_X, with the output offset resistor, R_A, equal to 10 kΩ. Note that the minimum detectable input signal, with $R_X = 0$, is approximately 100 mV, rms.

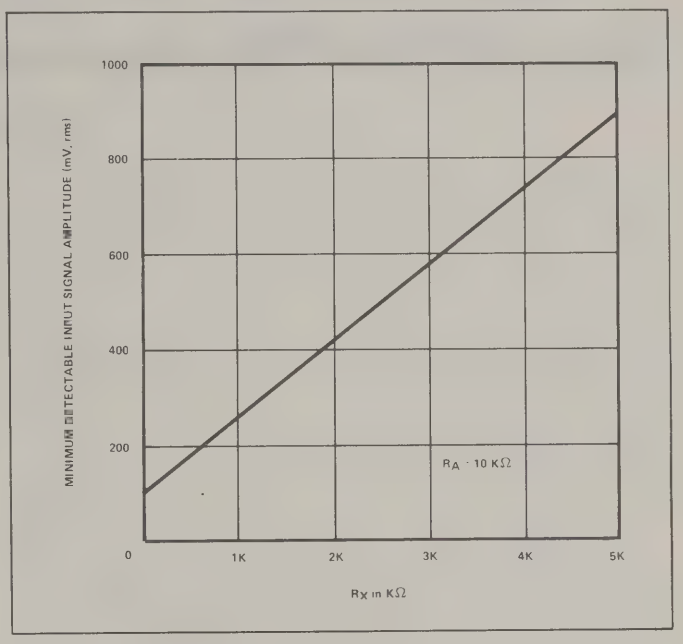


Figure 7. Minimum Detectable Input Carrier Level, as a Function of Multiplier Gain Setting Resistor, R_X.

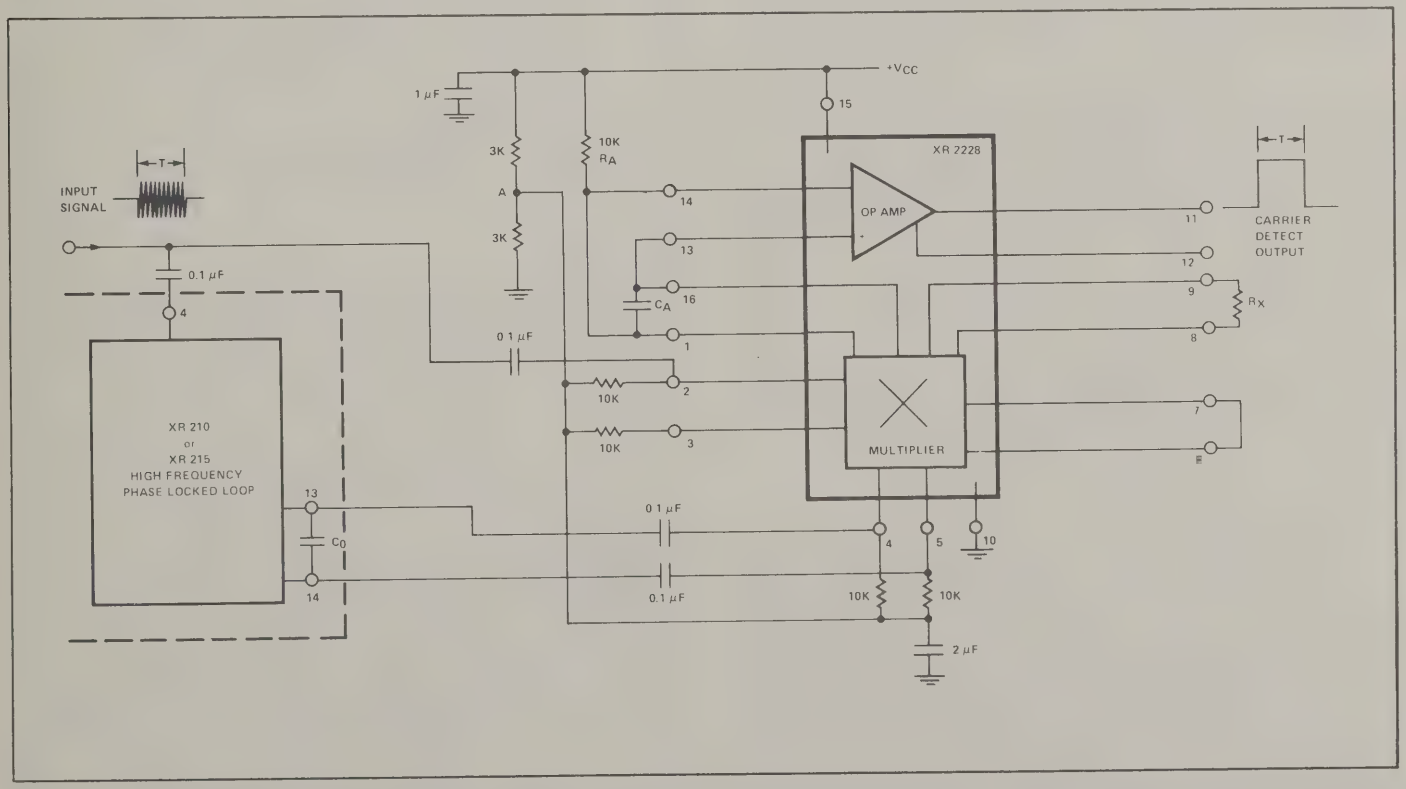


Figure 6. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone- or Carrier-Detector Application

Application Note AN-13

Frequency-Selective AM Detection Using Monolithic Phase-Locked Loops

INTRODUCTION

This application note describes the use of monolithic phase-locked loop (PLL) circuits in detection of amplitude-modulated (AM) signals. The detection capabilities of a PLL system, which is a frequency-selective FM demodulator, can be extended to cover AM signals simply by the addition of an analog multiplier (or mixer) and a low-pass filter to the basic phase-locked loop. This technique of AM demodulation, which is called "synchronous AM detection", offers significant performance advantages over conventional "peak-detector" type AM demodulators, in terms of its dynamic range and noise characteristics.

This application note outlines some of the fundamental principles of synchronous AM detectors, and gives design examples using the XR-2228 multiplier/detector IC in conjunction with the XR-215 and the XR-2212 monolithic PLL circuits.

PRINCIPLE OF OPERATION

The phase-locked loop AM detector circuits operate on the so-called "coherent AM detection" principle, where the amplitude modulated input signal is mixed with an unmodulated "coherent" carrier signal, and then low-pass filtered to produce the desired demodulated output signal. Figure 1 gives a simplified block diagram of such a detector system.

The amplitude-modulated input signal can be described by an expression of the form:

$$\text{Input Signal} = V_m(t) \cos \omega_0 t$$

where $V_m(t)$ is the modulated amplitude of the input signal and ω_0 is the input signal frequency expressed in radians. If this signal is linearly multiplied with an *unmodulated* signal which has the *same* frequency and phase as the input signal, then the output of the multiplier, $V_0(t)$, is a composite signal of the form:

$$V_0(t) = K_0 V_m(t) \left[1 + \cos (2 \omega_0 t)\right]$$

where K_0 is the gain of the multiplier circuit. If the above signal is then passed through a low-pass filter, to eliminate the double-frequency term, the resulting output signal is:

$$V_{out} = \text{Output Signal} = K_0 V_m(t)$$

which corresponds to the detected AM information.

The phase-locked loop AM detectors also operate on a similar principle: the PLL is made to "lock" on the carrier frequency of the input AM signal; then the VCO output of the PLL will regenerate the unmodulated coherent carrier signal necessary for detection. When this signal is mixed with the input AM signal and the resulting composite signal is passed through a low-pass filter, one obtains the demodulated output. Figure 2, gives a block diagram of such an AM detector system. Compared to the basic synchronous AM detector system of Figure 1, the phase-locked loop AM detector of Figure 2, also has one added feature: the output of the PLL control voltage (i.e., output of the PLL low-pass filter) can be used as an FM detector or a frequency discriminator. Thus, such a system is capable of simultaneous AM and FM detection. In other words, the frequency and the amplitude modulation information present on the input signal can be *separately* and *simultaneously* demodulated. The particular design and application examples given in this application note fall into this category.

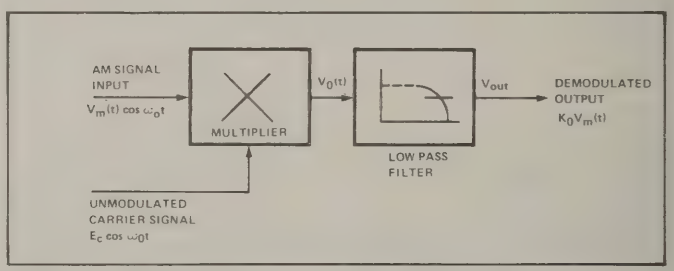


Figure 1. Block Diagram of a Synchronous AM Detector

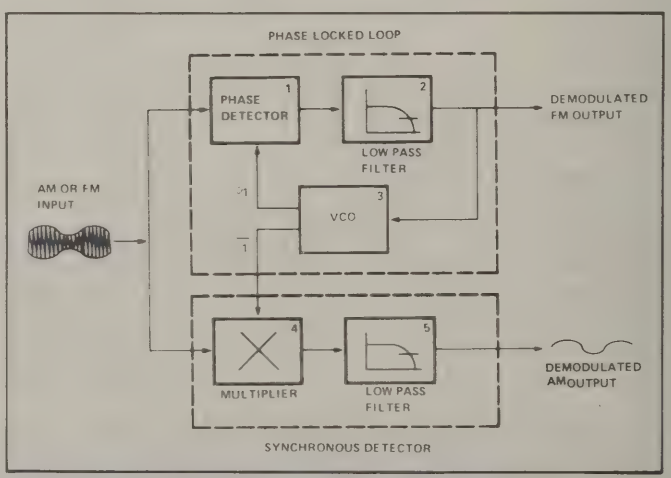


Figure 2. The Basic Phase-Locked Loop AM Detector

XR-2212 AND XR-2228 MONOLITHIC CIRCUITS

The XR-2212 monolithic PLL is made up of an input pre-amplifier, a phase-detector, a high-gain differential amplifier and a stable voltage-controlled oscillator (VCO) as shown in Figure 3. The key feature of the XR-2212 PLL is the temperature stability and the frequency accuracy of its VCO section; it offers 20 ppm/°C typical temperature stability and a frequency accuracy of ±1% for an external RC setting. The oscillator section of the XR-2212 contains a separate "quadrature output" terminal (pin 15) which is particularly intended for interfacing with a synchronous AM detector such as the XR-2228.

The XR-2228 multiplier/detector IC is specifically intended as a basic building block for synchronous AM detection. It contains a four-quadrant analog multiplier and a high-gain op amp on the same chip, as shown in the functional block diagram of Figure 4.

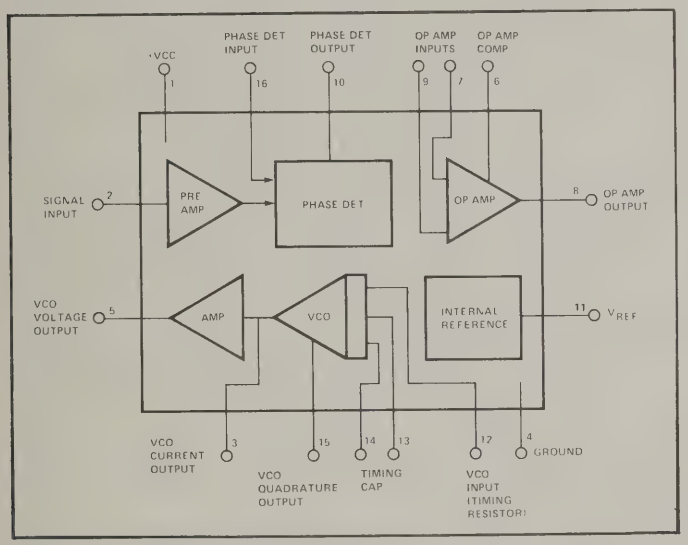


Figure 3. Functional Block Diagram of XR-2212 Precision Phase-Locked Loop

XR-215 HIGH FREQUENCY PHASE-LOCKED LOOP

The XR-215 is a high frequency phase-locked loop circuit capable of operating with input signal frequencies up to 35 MHz. It is comprised of a high frequency VCO, a phase-detector and an op amp section, as shown in the block diagram of Figure 5.

Unlike the XR-2212 PLL, the VCO section of the XR-215 does not have a separate "quadrature output" terminal. However, such a quadrature oscillator signal can be obtained by amplifying and "slicing" the triangle waveform available across the timing capacitor (pins 13 and 14) of the XR-215 oscillator section. Figure 6, shows the relative phase relationship of these oscillator waveforms available from the circuit. The desired quadrature output signal (Curve C of Figure 6) can be obtained by directly connecting one pair of the differential inputs of the XR-2228 directly across the timing capacitor terminals of the XR-215.

AM/FM DETECTION USING THE XR-2212 PLL

Figure 7, shows a generalized circuit connection diagram for a

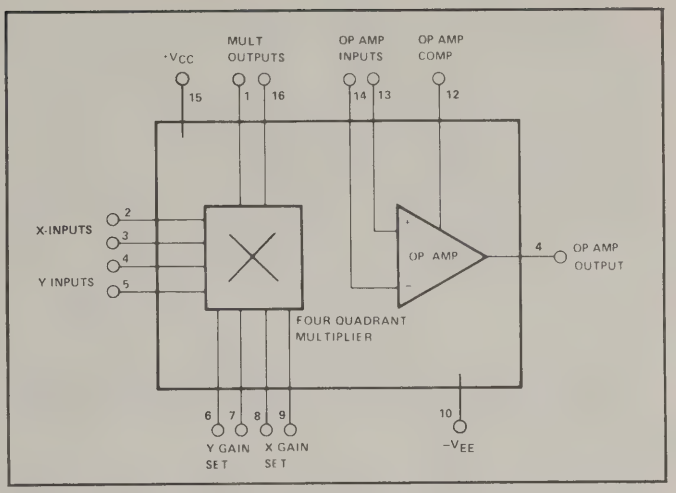


Figure 4. Functional Block Diagram of XR-2228 Multiplier/ Detector IC

two-chip AM and FM detection system, utilizing the XR-2212 PLL and the XR-2228 multiplier/detector. The XR-2212 section serves as the basic FM detector. The quadrature output of its VCO (pin 15) is AC coupled to the Y-input of the XR-2228.

The Y-input of the XR-2228 is operated in its switching mode, with the Y-gain terminals (pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; and all the multiplier inputs are DC biased from the internal reference output of the XR-2212 (pin 11). The output of the multiplier, at pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal.

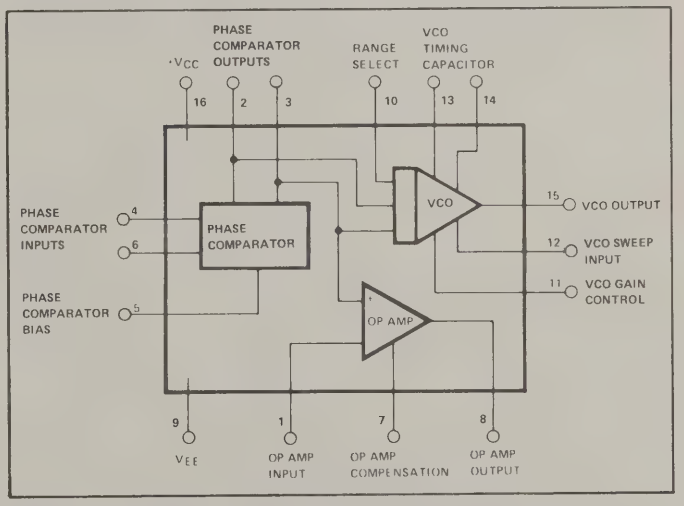


Figure 5. Functional Diagram of XR-215 High-Frequency Phase-Locked Loop

The circuit configuration shown in Figure 7, can operate with a single power supply, over the supply voltage range, of 10V to 20V. Its operation or performance can be tailored for any particular AM and FM detection application by the choice of external components shown in the figure, over a carrier frequency band of 1 kHz to 300 kHz. The functions of these external components are as follows:

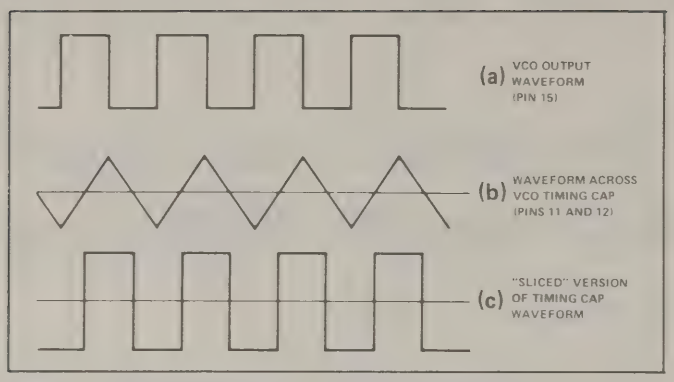


Figure 6. Timing Diagrams of VCO Output Waveforms from XR-215 Monolithic Phase-Locked Loop

a) R_0 and C_0 set the VCO center frequency for the XR-2212 PLL circuit. The center frequency, f_0 is given as:

$$f_0 = \frac{1}{R_0 C_0}$$

The VCO frequency f_0 is chosen to be equal to the carrier frequency of the input signal. R_0 is normally chosen to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. For most applications $R_0 \approx 20$ kΩ is recommended. Once f_0 is given and R_0 is chosen, then C_0 can be calculated from the above equation.

b) R_1 determines the tracking bandwidth of the PLL. For a required tracking bandwidth, Δf (see Figure 9 of XR-2212 data sheet) and f_0, R_1 can be calculated as:

$$R_1 = R_0\left(\frac{f_0}{\Delta f}\right)$$

This tracking bandwidth, Δf, is the band of frequencies in the vicinity of f_0, over which the PLL can maintain lock.

c) C_1 sets the loop-damping factor for the PLL. For most applications, C_1 is chosen to be equal to one-half of C_0.

d) R_2 and C_2 form a low-pass filter for the detected FM signal. The 3-dB frequencing, f_2, of this low-pass filter is:

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

Normally, f_2 is chosen to be equal to the demodulated FM information bandwidth.

e) R_C and R_{F1} set the gain of the op amp section of the XR-2212 as:

$$A_V = \left(1 + \frac{R_{F1}}{R_C}\right)$$

This op amp section serves as the post-detection amplifier for the demodulated FM signals.

f) R_X sets the multiplier gain for the X-input and R_{F2} sets the gain of the op amp section of the XR-2228. Thus, the demodulated AM signal output swing, V_{out}, for a given input signal of peak amplitude of V_M and modulation index of m ($0 \leq m \leq 1$) can be approximated as:

$$V_{out} = \frac{(V_M)_m}{4}\left(\frac{R_{F2}}{R_X}\right)$$

Thus, for example, a 100 mV peak input signal with 30% AM modulation (m = 0.3) will give a demodulated output of 150 mV peak, with R_{F2} = 100 kΩ and R_X = 5 kΩ, at pin 11 of the XR-2228.

g) C_3, in conjunction with the 5 kΩ internal impedance of the multiplier output (pin 16) serves as the low-pass post-detection filter for the demodulated AM signal.

For further explanation and description of the system design equations, the reader is referred to the XR-2212 and the XR-2228 data sheets.

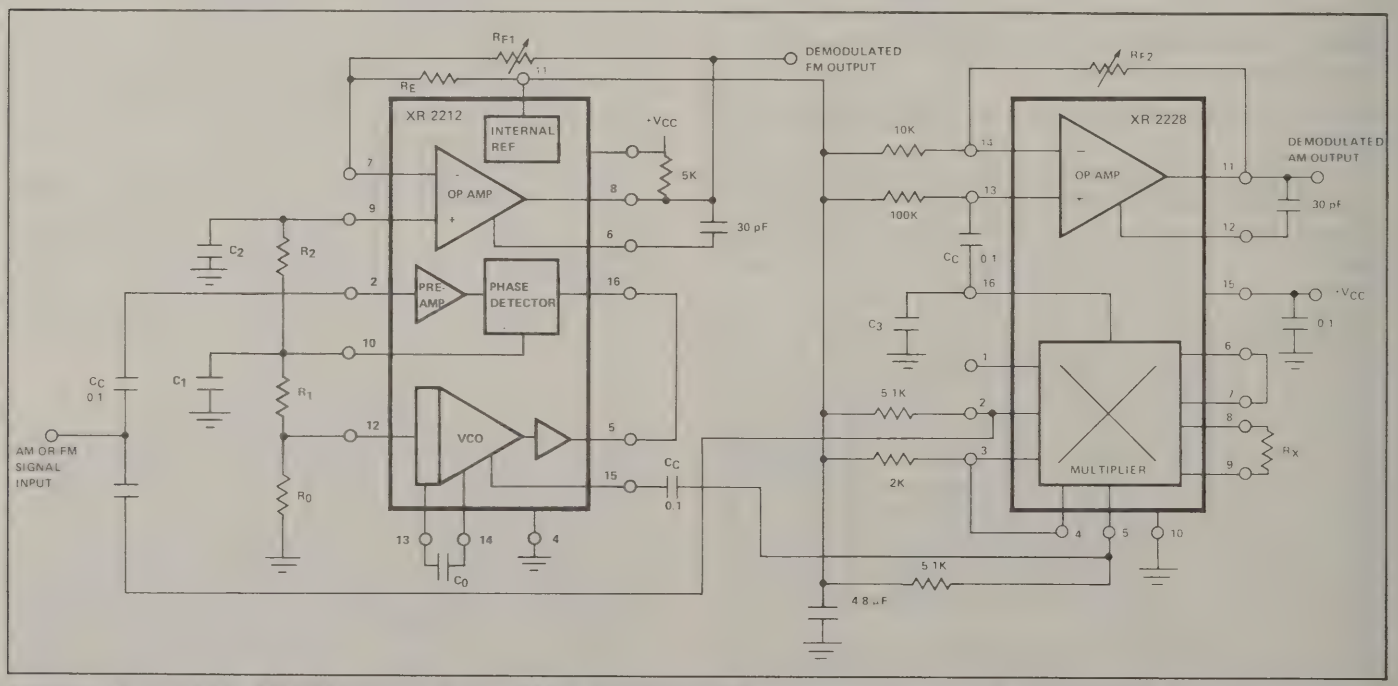


Figure 7. A Two-Chip AM/FM Detector System Using the XR-2212 Phase-Locked Loop and the XR-2228 Multiplier/Detector

Design Example: Design an AM demodulator for 100 kHz carrier frequency with a detection (tracking) bandwidth of ±4%. The demodulated information bandwidth is 3 kHz and an output level of 1 volt peak is required for a 1 volt peak input with 30% modulation.

Using the circuit of Figure 7, one proceeds as follows: Since FM detection is not required in this example, components R_2, C_2, R_C and R_{F1} are not essential to circuit operation. R_2 and R_C can be short-circuited, C_2 and R_{F1} can be left open-circuited. The rest of the component values are calculated as follows:

Step 1) Set f_0 = 100 kHz by choosing R_0 = 20 kΩ and calculating C_0 from paragraph (a) above:

$$C_0 = \frac{1}{R_0 f_0} = 500 \text{ pF}$$

Step 2) Determine R_1 to set tracking bandwidth to ±4%, from paragraph (b): R_1 = 500 kΩ

Step 3) Calculate C_1: $C_1 \approx C_0/2 \approx 250$ pF

Step 4) From paragraph (f), calculate the value of R_X and R_{F2}. For a typical choice of R_X = 5 kΩ, and m = 0.3 (30% modulation) with 1 volt input carrier level, the value of R_{F2} to get 1 volt demodulated output is: R_{F2} = 67 kΩ

Step 5) Calculate C_3 to get 3 kHz bandwidth for post-detection filter: $C_3 \approx 0.01$ μF

AM DETECTION USING THE XR-215 PLL

Figure 8, shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit of Figure 8, is useful as a phase-locked AM detector for carrier frequencies up to 20 MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate "quadrature" output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (pins 13 and 14) of XR-215. The Y-input of the XR-2228 is operated with maximum gain, since the Y-gain control terminals (pins 6 and 7) are shorted together. This causes the triangular waveform across C_0 to be converted to an effective "quadrature" drive as indicated by the timing diagram of Figure 6. The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X-inputs of the XR-2228, are biased at approximately one-half of V_{CC}, by means of an external resistive divider.

In Figure 8, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier.

The mode of operation of the XR-2228 is virtually the same as that described in connection with Figure 7: R_X sets the multiplier demodulation gain; C_3 serves as the low-pass post-detection filter. The values of R_X, R_{F2} and C_3 are calculated as given in paragraphs (f) and (g).

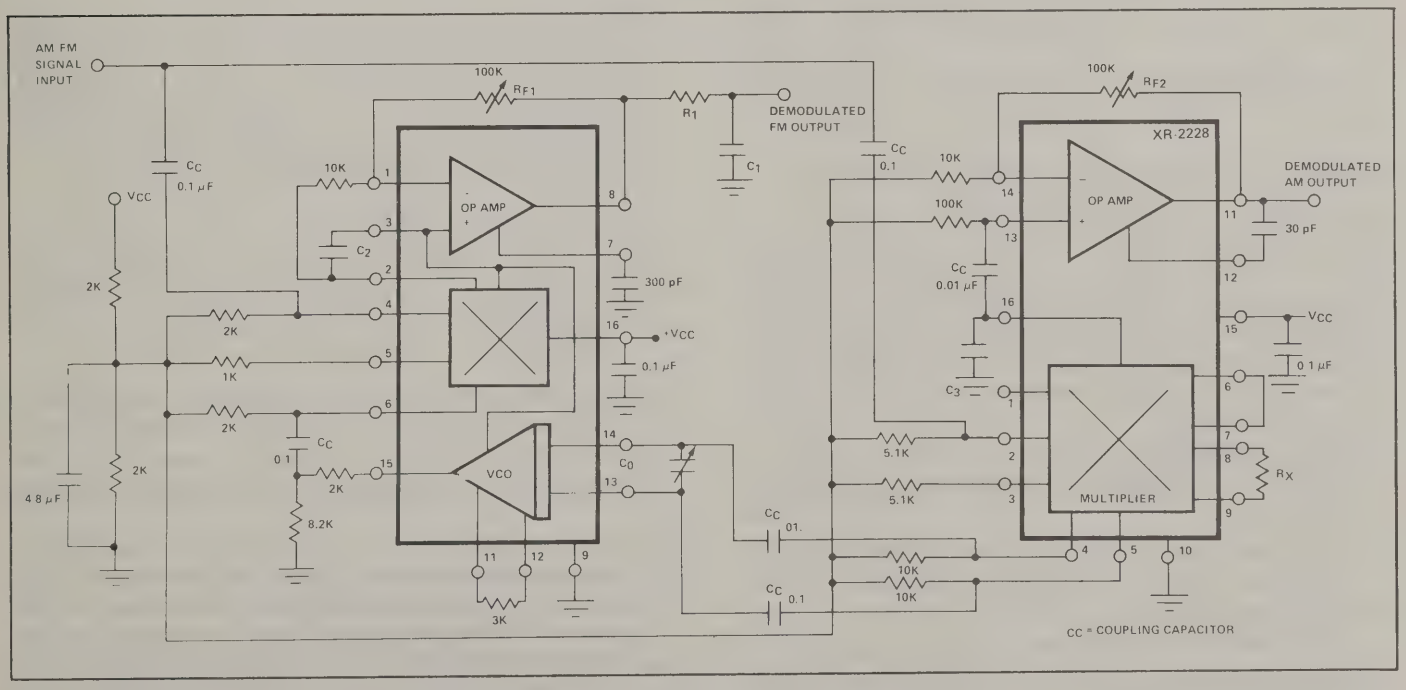


Figure 8. Circuit Connection for a High-Frequency AM and FM Detector Using the XR-215 and the XR-2228

Application Note AN-14

A High Quality Function Generator System Using the XR-2206

INTRODUCTION

Waveform or function generators capable of producing AM/FM modulated sine wave outputs find a wide range of applications in electrical measurement and laboratory instrumentation. This application note describes the design, construction and the performance of such a complete function generator system suitable for laboratory usage or hobbyist applications. The entire function generator is comprised of a single XR-2206 monolithic IC and a limited number of passive circuit components. It provides the engineer, student, or hobbyist with highly versatile laboratory instrument for waveform generation at a very small fraction of the cost of conventional function generators available today.

GENERAL DESCRIPTION

The basic circuit configuration and the external components necessary for the high-quality function generator system is shown in Figure 1. The circuit shown in the figure is designed to operate with either a 12V single power supply, or with a ±6V split supplies. For most applications, split-supply operation is preferred since it results in an output DC level which is nearly at ground potential.

The circuit configuration of Figure 1 provides three basic waveforms: sine, triangle and square wave. There are four overlapping frequency ranges which give an overall frequency range of 1 Hz to 100 kHz. In each range, the frequency may be varied over a 100:1 tuning range.

The sine or triangle output can be varied from 0 to over 6V (peak to peak) from a 600 ohm source at the output terminal.

A squarewave output is available at the sync output terminal for oscilloscope synchronizing or driving logic circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

The performance characteristics listed below are not guaranteed or warranted by Exar. However, they represent the typical performance characteristics measured by Exar's application engineers during the laboratory evaluation of the function generator system shown in Figure 1. The typical performance specifications listed below apply *only* when all of the recommended assembly instructions and adjustment procedures are followed:

(a) **Frequency Ranges**: The function generator system is designed to operate over four overlapping frequency ranges:

1 Hz to 100 Hz
10 Hz to 1 kHz
100 Hz to 10 kHz
1 kHz to 100 kHz

The range selection is made by switching in different timing capacitors.

(b) **Frequency Setting**: At any range setting, frequency can be varied over a 100:1 tuning range with a potentiometer (see R_{13} of Figure 1).

(c) **Frequency Accuracy**: Frequency accuracy of the XR-2206 is set by the timing resistor R and the timing capacitor C, and is given as:

$$f = 1/RC$$

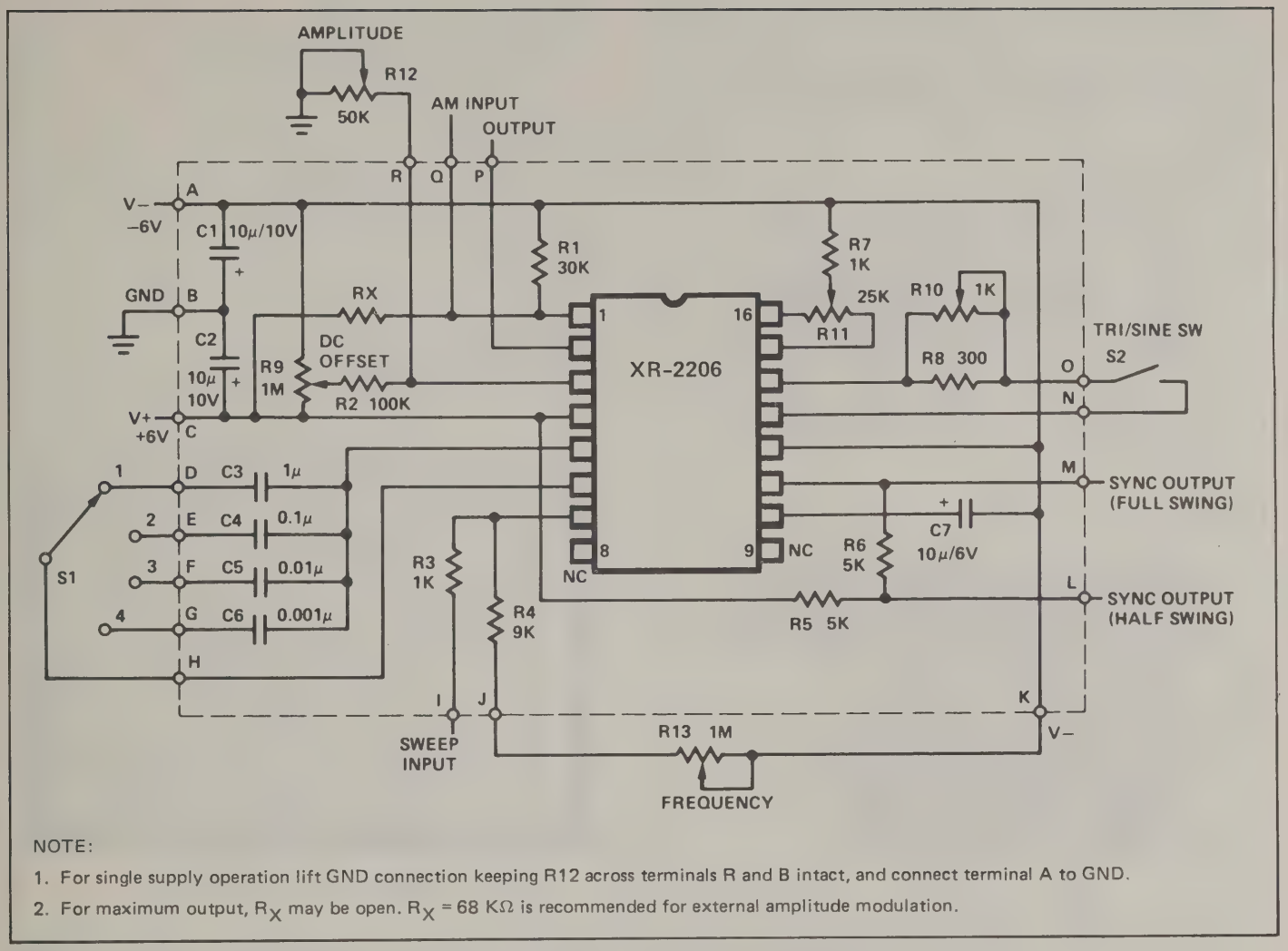
The above expression is accurate to within ±5% at any range setting. The timing resistor R is the series combination of resistors R_4 and R_{13} of Figure 1. The timing capacitor C is any one of the capacitors C_3 through C_6, shown in the figure.

(d) **Sine and Triangle Output**: The sine and triangle output amplitudes are variable from 0V to 6 V_{pp}. The amplitude is set by an external potentiometer, R_{12} of Figure 1. At any given amplitude setting, the triangle output amplitude is approximately twice as high as the sinewave output. The internal impedance of the output is 600Ω.

(e) **Sinewave Distortion**: The total harmonic distortion of sinewave is less than 1% from 10 Hz to 10 kHz and less than 3% over the entire frequency range. The selection of a waveform is made by the triangle/sine selector switch, S_2.

(f) **Sync Output**: The sync output provides a 50% duty cycle pulse output with either full swing or upper half swing of the supply voltage depending on the choice of sync output terminals on the printed circuit board (see Figure 1).

(g) **Frequency Modulation (External Sweep)**: Frequency can be modulated or swept by applying an external control voltage to sweep terminal (Terminal I of Figure 1). When not used, this terminal should be left open-circuited. The open circuit voltage at this terminal is approximately 3V above the negative supply voltage and its impedance is approximately 1000 ohms.



NOTE:

1. For single supply operation lift GND connection keeping R12 across terminals R and B intact, and connect terminal A to GND.
2. For maximum output, R_X may be open. R_X = 68 KΩ is recommended for external amplitude modulation.

Figure 1. Circuit Connection Diagram for Function Generator. (See Note 1 for single supply operation.)

(h) **Amplitude Modulation (AM):** The output amplitude varies linearly with modulation voltage applied to AM input (terminal Q of Figure 1). The output amplitude reaches its minimum as the AM control voltage approaches the half of the total power supply voltage. The phase of the output signal reverses as the amplitude goes through its minimum value. The total dynamic range is approximately 55 dB, with AM control voltage range of 4V referenced to the half of the total supply voltage. When not used, AM terminal should be left open circuited.

(i) **Power Source:** Split supplies: ±6V, or single supply: +12V. Supply Current: 15 mA (see Figure 3).

EXPLANATION OF CIRCUIT CONTROLS:

Switches

Range Select Switch, S1: Selects the frequency range of operation for the function generator. The frequency is inversely proportional to the timing capacitor connected across Pins 5 and 6 of the XR-2206 circuit. Nominal capacitance values and frequency ranges corresponding to switch positions of S1 are as follows:

Position	Nominal Range	Timing Capacitance
1	1 Hz to 100 Hz	1 μF
2	10 Hz to 1 kHz	0.1 μF
3	100 Hz to 10 kHz	0.01 μF
4	1 kHz to 100 kHz	0.001 μF

If additional frequency ranges are needed, they can be added by introducing additional switch positions.

Triangle/Sine Waveform Switch, S2: Selects the triangle or sine output waveform.

Trimmers and Potentiometers

DC Offset Adjustment, R9: The potentiometer used for adjusting the DC offset level of the triangle or sine output waveform.

Sinewave Distortion Adjustment, R10: Adjusted to minimize the harmonic content of sinewave output.

Sinewave Symmetry Adjustment, R11: Adjusted to optimize the symmetry of the sinewave output.

Amplitude Control, R12: Sets the amplitude of the triangle or sinewave output.

Frequency Adjust, R13: Sets the oscillator frequency for any range setting of S1. Thus, R13 serves as a frequency dial on a conventional waveform generator and varies the frequency of the oscillator over an approximate 100 to 1 range.

Terminals

A. Negative Supply –6V
B. Ground
C. Positive Supply +6V
D. Range 1, timing capacitor terminal
E. Range 2, timing capacitor terminal
F. Range 3, timing capacitor terminal
G. Range 4, timing capacitor terminal
H. Timing capacitor common terminal
I. Sweep Input
J. Frequency adjust potentiometer terminal
K. Frequency adjust potentiometer negative supply terminal
L. Sync output (1/2 swing)
M. Sync output (full swing)
N. Triangle/sine waveform switch terminals
O. Triangle/sine waveform switch terminals
P. Triangle or sinewave output
Q. AM input
R. Amplitude control terminal

PARTS LIST

The following is a list of external circuit components necessary to provide the circuit interconnections shown in Figure 1.

Capacitors:

C1, C2, C7	Electrolytic, 10 μF, 10V
C3	Mylar, 1 μF, nonpolar, 10%
C4	Mylar, 0.1 μF, 10%
C5	Mylar, 0.01 μF, 10%
C6	Mylar, 1000 pF, 10%

Resistors:

R1	30 KΩ, 1/4W, 10%
R2	100 KΩ, 1/4W, 10%
R3, R7	1 KΩ, 1/4W, 10%
R4	9 KΩ, 1/4W, 10%
R5, R6	5 KΩ, 1/4W, 10%
R8	300Ω, 1/4W, 10%
RX	62 KΩ, 1/4 W, 10% (RX can be eliminated for maximum output)

Potentiometers:

R9	Trim, 1 MΩ, 1/4W
R10	Trim, 1 KΩ, 1/4W
R11	Trim, 25 KΩ, 1/4W

The following additional items are recommended to convert the circuit of Figure 1 to a complete laboratory instrument:

Potentiometers:

R12	Amplitude control, linear, 50 KΩ
R13	Frequency control, audio taper, 1 MΩ

Switches:

S1	Rotary switch, 1-pole, 4 pos.
S2	Toggle or slide, SPST

Case:

7" x 4" x 4" (approx.) Metal or Plastic
(See Figures 4(a) and 4(b).)

Power Supply:

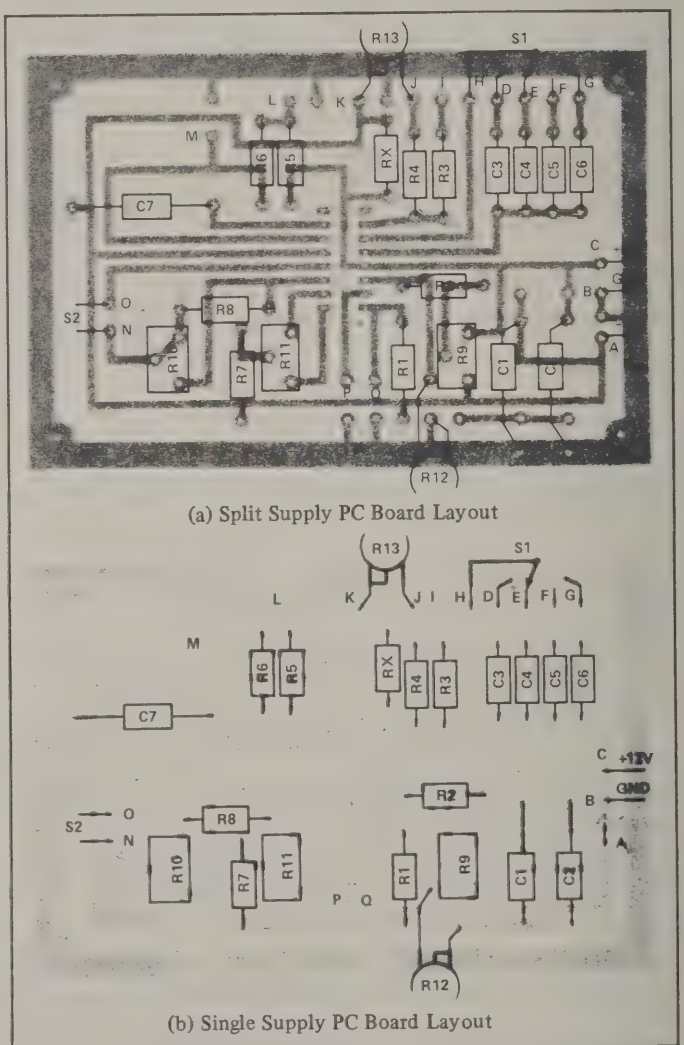
Dual supplies ±6V or single +12V
Batteries or power supply unit
(See Figures 3(a) and 3(b).)

Miscellaneous:

Knobs, solder, wires, terminals, etc.

BOARD LAYOUT

Figures 2(a) and 2(b) show the recommended printed-circuit board layout for the function generator circuit of Figure 1.



(a) Split Supply PC Board Layout

(b) Single Supply PC Board Layout

Figure 2. Recommended PC Board Layout for Function Generator Circuit of Figure 1.

RECOMMENDED ASSEMBLY PROCEDURE

The following instructions and recommendations for the assembly of the function generator assume that the basic PC board layout of Figures 2(a) or 2(b) is used in the circuit assembly.

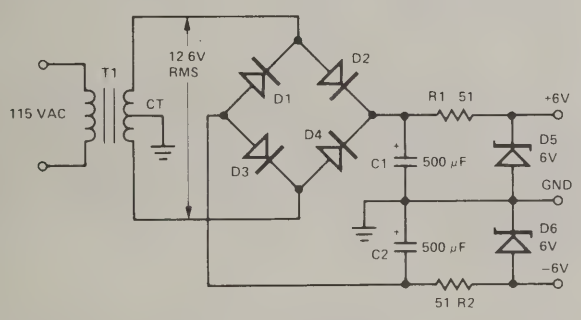
All the parts of the generator, with the exception of frequency adjust potentiometer, amplitude control potentiometer, triangle/sine switch and frequency range select switch, are mounted on the circuit board.

Install and solder all resistors, capacitors and trimmer resistors on the PC board first. Be sure to observe the polarity of capacitors C1, C2 and C7. The timing capacitors C3, C4, C5 and C6 must be non-polar type. Now install IC1 on the board. We recommend the use of an IC socket to prevent possible damage to the IC during soldering and to provide for easy replacement in case of a malfunction.

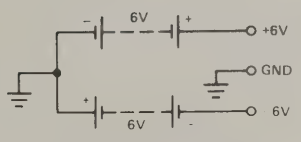
The entire generator board along with power supply or batteries and several switches and potentiometers will fit into a case of the type readily available at electronic hobby shops. It will be necessary to obtain either output jacks or terminals for the outputs and AM and frequency sweep inputs.

Install the frequency adjust pot, the frequency range select switch, the output amplitude control pot, the power switch, and the triangle/swine switch on the case. Next, install the PC board in the case, along with a power supply.

Any simple power supply having reasonable regulation may be used. Figure 3 gives some recommended power supply configuration.



(a) Zener Regulated Supply



(b) Battery Power Supply

T1: Filament transformer
Primary 115V/Secondary 12.6 VCT, 0.5A
D1 – D4: IN4001 or similar
D5, D6: IN4735 or similar
C1, C2: Electrolytic, 500 μF/12 VDC
R1, R2: 51Ω, 1/2W, 10%

Figure 3. Recommended Power Supply Configurations.

Precaution: Keep the lead lengths small for the range selector switch.

Figure 4 gives an example of the fully assembled version of the function generator system described above.

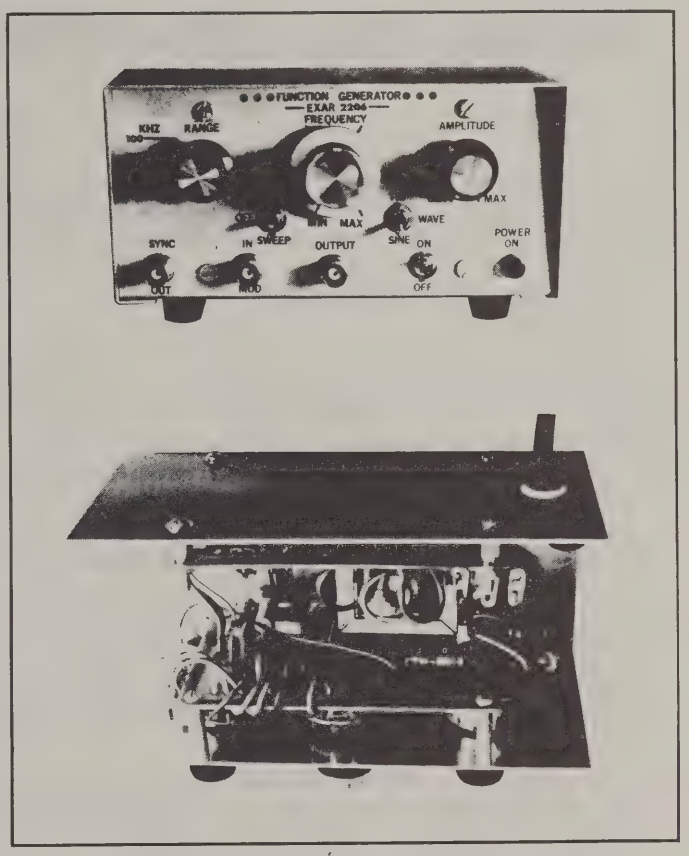


Figure 4. Typical Example of a Fully Assembled Function Generator.

ADJUSTMENT PROCEDURE

When assembly is completed and you are ready to put the function generator into operation, make sure that the polarity of power supply and the orientation of the IC unit are correct. Then apply the DC power to the unit.

To adjust for minimum distortion, connect the scope probe to the triangle/sine output. Close S2 and adjust the amplitude control to give non-clipping maximum swing. Then adjust R10 and R11 alternately for minimum distortion by observing the sinusoidal waveform. If a distortion meter is available, you may use it as a final check on the setting of sine-shaping trimmers. The minimum distortion obtained in this manner is typically less than 1% from 1 Hz to 10 kHz and less than 3% over the entire frequency range.

Application Note AN-15

An Electronic Music Synthesizer Using the XR-2207 and the XR-2240

INTRODUCTION

This application note describes a simple, low-cost "music synthesizer" system made up of two monolithic IC's and a minimum number of external components. The electronic music synthesizer is comprised of the XR-2207 programmable tone generator IC which is driven by the pseudo-random binary pulse pattern generated by the XR-2240 monolithic counter/timer circuit.

PRINCIPLE OF OPERATION

All the active components necessary for the electronic music synthesizer system is contained in the two low-cost monolithic IC's, the XR-2207 variable frequency oscillator and the XR-2240 programmable counter/timer. Figure 1 shows the functional block diagram of the XR-2207 oscillator. This monolithic IC is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and square-wave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The XR-2240 programmable counter/timer is comprised of an internal time-base oscillator, a control flip-flop and a programmable 8-bit binary counter. Its functional block diagram is shown in Figure 2, in terms of the 16-pin IC package. The eight separate output terminals of the XR-2240 are "open-collector" type outputs which can either be used individually, or can be connected in a "wired-or" configuration.

Figure 3 shows the circuit connection for the electronic music or time synthesizer system using the XR-2207 and the XR-2240. The XR-2207 produces a sequence of tones by oscillating at a frequency set by the external capacitor C_1 and the resistors R_1 through R_6 connected to Pins 4 through 17. These resistors set the frequency or the "pitch" of the output tone sequence. The counter/timer IC generates the pseudo-random pulse patterns by selectively counting down the time-base frequency. The counter outputs of XR-2240 (Pins 1 through 8) then activate the timing resistors R_1 through R_6 of the oscillator IC, which converts the binary pulse patterns to tones. The time-base oscillator frequency of the counter/timer sets the "beat" or the tempo of the music. This setting is done through C_3 and R_0 of Figure 3.

The pulse sequence coming out of the counter/timer IC can be programmed by the choice of counter outputs (Pins 1 through 8 of XR-2240 connected to the programming pins (Pins through 7) of the XR-2207 VCO. The connection of Figure 3 is recommended since it gives a particularly melodic tone sequence at the output.

The pseudo-random pulse pattern out of the counter-timer repeats itself at 8-bit (or 256 count) intervals of the time-base period. Thus, the output tone sequence continues for about 1 to 2 minutes (depending on the "beat") and then repeats itself. The counter/timer resets to zero when the device is turned on; thus, the music, or the tone sequence, always starts from the same point when the synthesizer is turned on.

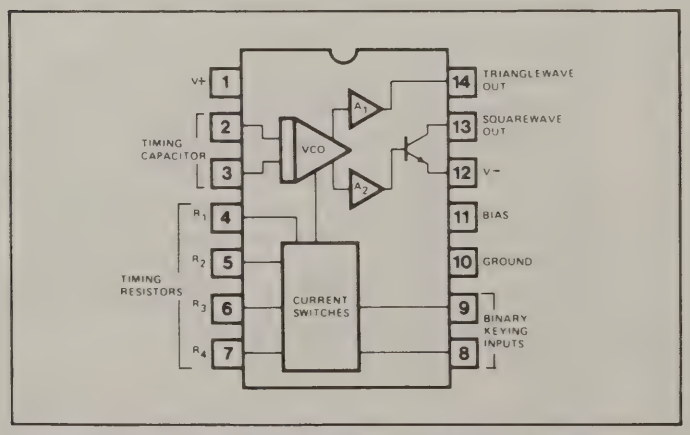


Figure 1. Functional Block Diagram of XR-2207 Oscillator Circuit.

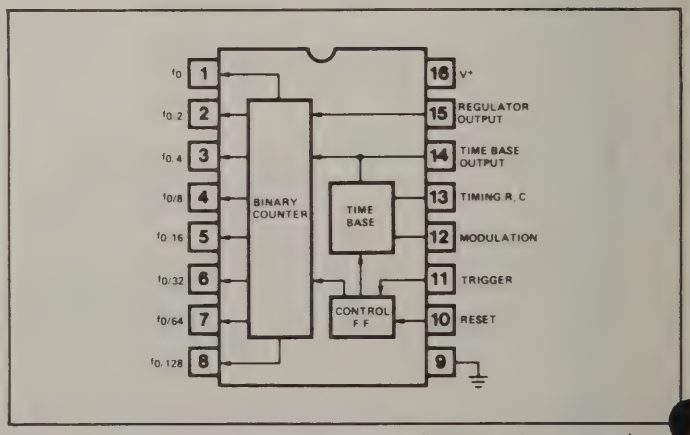


Figure 2. Functional Block Diagram of XR-2240 Counter/Timer.

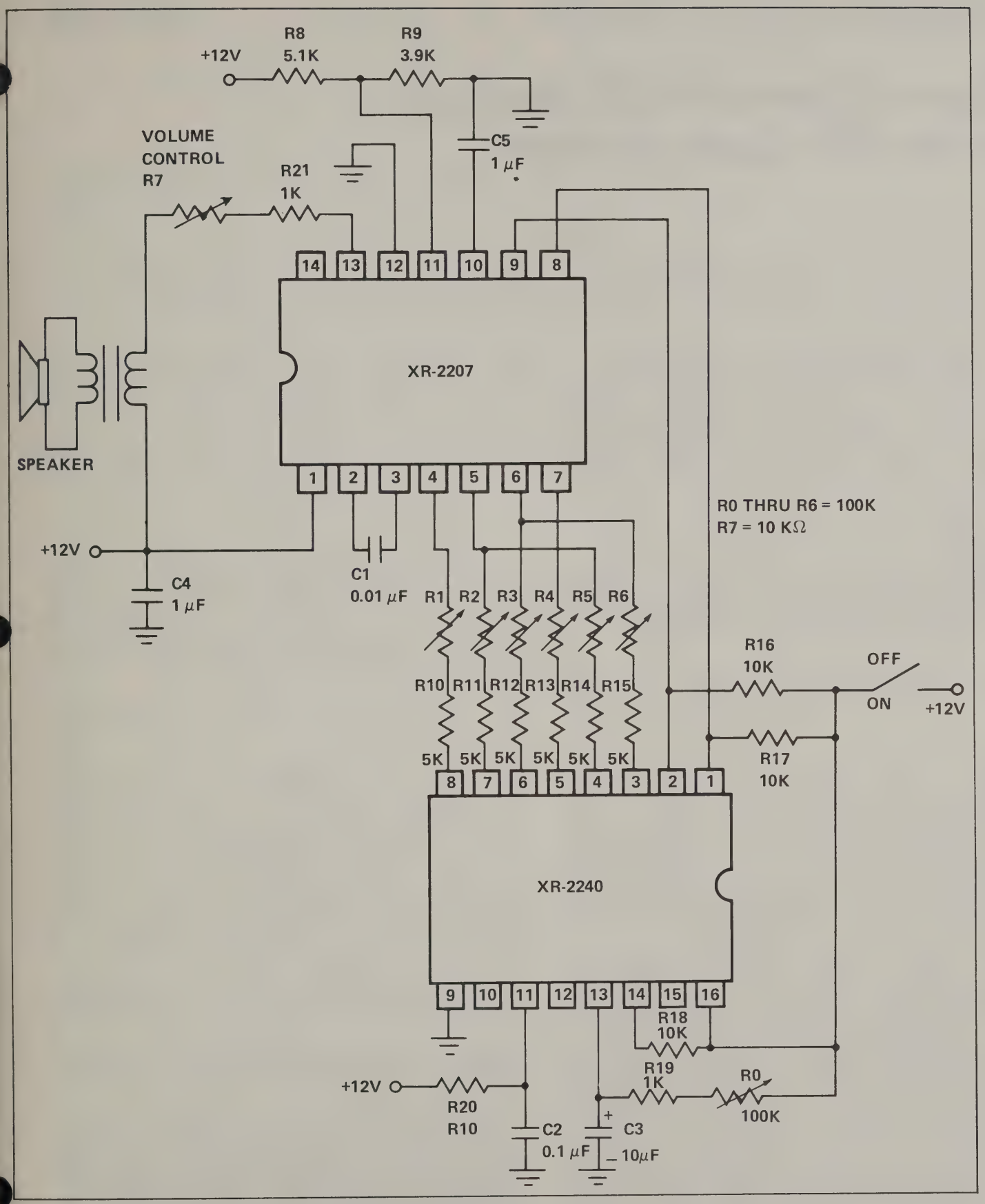


Figure 3. Circuit Connection Diagram for the Music Synthesizer.

Application Note AN-16

Semi-Custom LSI Design with I^2L Gate Arrays

INTRODUCTION

In designing semi-custom monolithic LSI, one uses a partially fabricated silicon wafer which is "customized" by the application of one or more special mask patterns. This technique greatly reduces the design and tooling cost and the prototype fabrication cycle associated with the conventional *full-custom IC* development cycle; and thus makes custom IC's economically feasible even at low production volumes.

Until recently, the application of semi-custom design technology to complex digital systems has been somewhat limited due to one key factor: to be economically feasible, a complex digital LSI chip must achieve a high functional density on the chip (i.e., high gate count per unit chip area). Traditionally, this requirement is not compatible with the random interconnection concept which is key to the semi-custom or master-slice design approach. This paper describes a *new* approach to the master-slice concept which overcomes this age-old problem. It achieves packing densities approaching those of full-custom digital LSI layout while still maintaining the low-cost and the quick turn-around attributes of semi-custom IC design. This is achieved by making use of unique layout and interconnection properties of I^2L gates, and by extending the mask-programming to additional mask layers besides the metal interconnection.

FEATURES OF I^2L TECHNOLOGY

Integrated Injection Logic (I^2L) is one of the most significant recent advances in the area of monolithic LSI technology. Compared to other monolithic LSI technologies, I^2L offers the following unique advantages:

- High Packing Density
- Bipolar Compatible Processing
- Low Power and Low Voltage Operation
- Low (Power x Delay) Product

Figure 1 gives a comparison of the speed and power capabilities of various logic families, including I^2L. Since I^2L technology is a direct extension of the conventional bipolar IC technology, it readily lends itself to combining high-density digital functions on the same chip along with conventional Schottky-bipolar circuitry. The availability of bipolar input-output interface on the same chip along with the high-density I^2L logic makes it very convenient to retrofit custom I^2L designs into many existing logic systems.

The I^2L logic technology is developed around the basic single-input, multiple-output inverter circuit shown in Figure 2. A recommended circuit symbol for this gate circuit is also defined in the figure. Most terminals of the I^2L gate share the same semi-conductor region (for example, the collector of the PNP is the same as the base of the NPN; and the emitter of the NPN is the same as the base of the PNP). This leads to a very compact device structure, and results in very high packing density in monolithic device fabrication. Figure 3 illustrates the basic device structure and the cross-section for a bipolar-compatible I^2L gate. Since the individual I^2L gates do not require separate P-type isolation diffusions, they can be placed in a common N-type tub. This feature greatly enhances the packing density on the chip since it eliminates the need for separate isolation pockets for individual gates. With conventional photo-masking and diffusion tolerances, gate densities of greater than 200 gates/mm^2 can be readily achieved in full-custom layout. Using the semi-custom approach which is outlined in this paper, one can maintain a packing density of

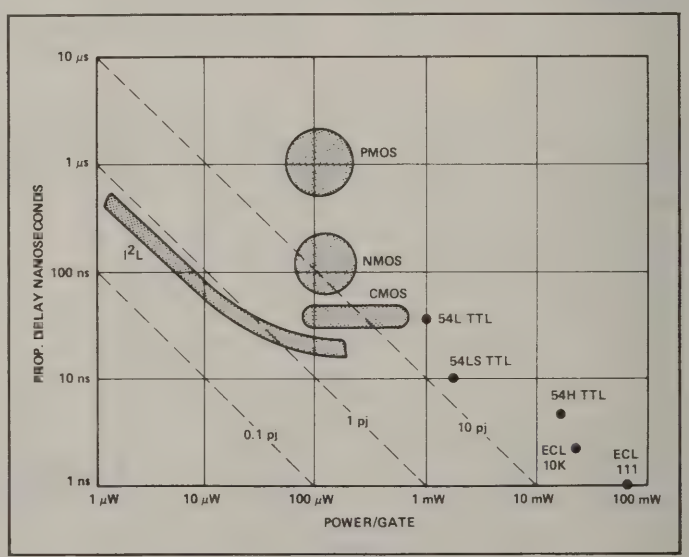


Figure 1. Comparison of Speed and Power Capabilities of Various Logic Families.

greater than 120 gates/mm^2 even with random metallization or interconnection requirements. This offers at least a factor of four improvement over conventional bipolar master-slice technology and approximately a factor of two improvement over MOS master-slice approach in terms of gate-density and chip area utilization.

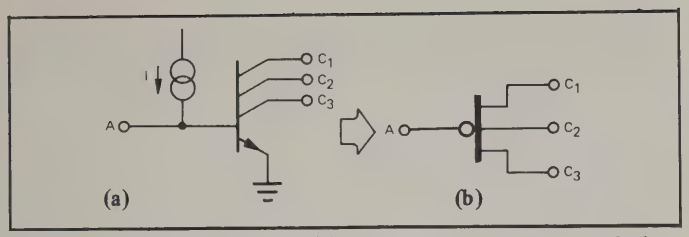


Figure 2. Equivalent Circuit (a), and a recommended symbol (b) for an I^2L Gate.

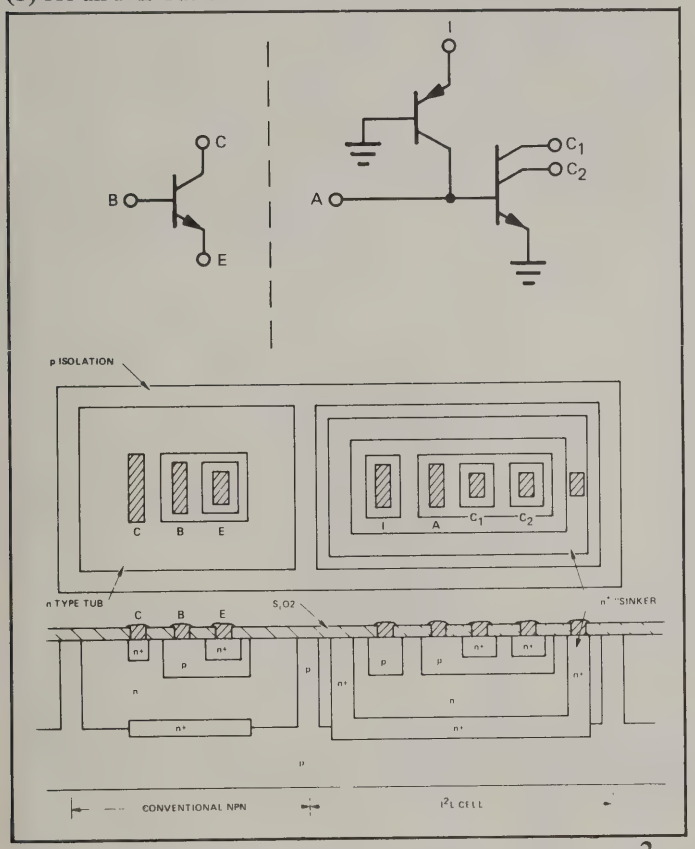


Figure 3. Basic Device Structure for Bipolar Compatible I^2L.

DESIGNING WITH I^2L GATE ARRAYS

A number of I^2L gate arrays have been developed at Exar utilizing bipolar-compatible integrated injection logic technology. The most recent additions to this family of products are the XR-300 and the XR-500 gate array chips which are specifically intended for semi-custom IC designs involving complex digital systems. These chips contain a large number of multiple-output I^2L gates along with Schottky-bipolar input/output buffers. Table I gives a summary of the components available on each of these chips.

Figure 4 shows the basic layout architecture of the XR-300 and the XR-500 gate array chips. As indicated in the figure, each chip is made up of two sections: (a) the I^2L gate matrix; and (b) the Schottky-bipolar input/output interface. In addition, the bipolar I/O section contains two identical sets of resistor arrays, located at opposite ends of the chip, which are used for biasing the injectors of the I^2L gates. The basic features of each of the sections of the gate array chips are outlined below:

TABLE 1

List of Components on XR-300 and XR-500 Semi-Custom Chips

COMPONENT TYPE	Chip Type XR-300	XR-500
Multiple Output I^2L Gates	288	520
Input/Output Buffers	28	40
Schottky – NPN Transistors	56	80
Resistors	168	240
Bonding Pads	34	42
Chip Size (mils)	104x140	122x185

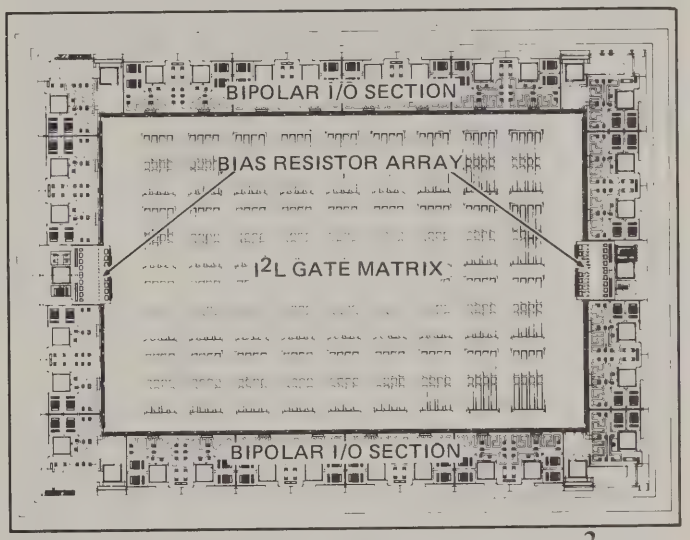


Figure 4. Basic Architecture of XR-300 and XR-500 I^2L Gate Arrays.

a) The I^2L Gate Matrix:

This section of the I^2L gate array is made up of 8-gate "cells." These cells contain eight multiple-output I^2L inverters which share a common set of four injectors. Figure 5 shows a basic 8-gate cell section within the I^2L gate section, prior to customization. The basic 8-gate cells forming the I^2L gate matrix are made up of P-type injectors and gate *fingers* which serve as the base regions of the I^2L gates. The six dots on each gate area indicate the possible locations or sites for gate input or outputs. The particular use of these sites as an input or an output is determined by two custom masks: an N-type collector diffusion mask which defines the locations of outputs, and a custom contact mask which opens the appropriate input and output contact. Finally, a third custom mask is applied to form the metal interconnections between the gates, and the gate cells. The custom N-type diffusion step, which determines the locations of gate outputs, is also used for forming low-resistivity underpasses between the gate-cells. The area between each of the gate cells can accomodate two or three parallel underpasses in the horizontal and the vertical directions, respectively. Since the N-type diffusion which forms these underpasses is a part of the customizing step, the location and the length of each underpass can be chosen to fit a given interconnection requirement. This method

provides the designer with virtually all the advantages and capabilities of multi-layer interconnection paths on the surface of the chip; and allows approximately 80% of the gates on the chip to be utilized in a typical random-logic layout.

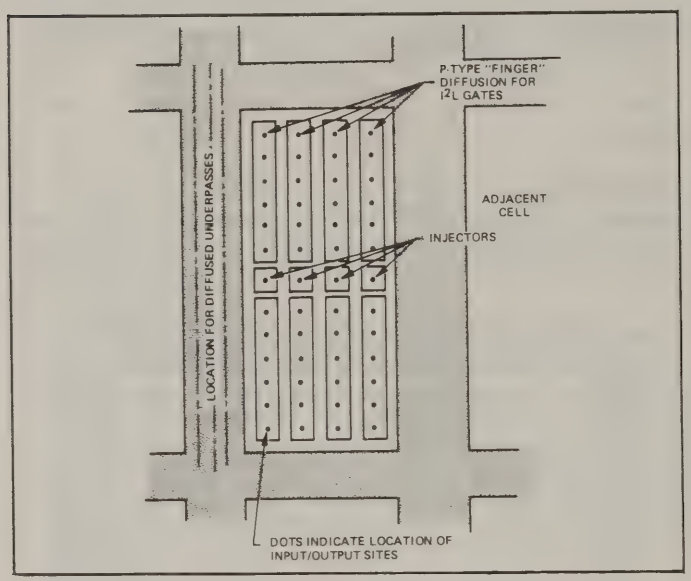


Figure 5. Basic 8-Gate Cell Before Customization.

The custom logic interconnections can be easily laid out in pencil on a layout sheet by simply interconnecting the desired gate "sites" with a pencil line and appropriately defining the function of the site as an input, output, injector contact or an underpass. Figure 6 shows a typical example of such a logic layout. The corresponding symbols defining the function of the sites on the layout are also identified in the figure. For convenience, an underpass is indicated with a resistor symbol, connecting two triangles corresponding to the terminal points of the underpass.

Figure 7 shows the sample layout of the same 8-gate cell, after its customization with a selective N-type collector diffusion, contact-window cut and the metal interconnection patterns.

Typical electrical characteristics of the I^2L gates within the gate matrix are listed in Table 2. Typical operating characteristics of the gates are given in Figures 8, 9 and 10, as a function of the injector current per gate. As indicated in Figure 8, the average power-delay product for a four-output gate is approximately 0.5 pJ at low currents; and the typical propagation delay, t_{pd}, at injector currents in excess of 100 μA/gate is approximately 50 nsec for the output furthest from the injector. Figure 9 shows the two components of the total propagation delay, namely the turn-on and turn-off delay, as a function of the injector bias. At low injector currents (i.e., $I_j \leq 10\ \mu A$), turn-on delay is the dominant factor. For high-speed operation with $I_j \geq 50\ \mu A$, turn-off delay becomes the dominant limitation in speed. Typical toggle rate of a D-type flip-flop as a function of injector current is shown in Figure 10. As indicated in the figure, toggle rates of 3 MHz are obtained at injector current levels of approximately 100 μA per gate.

TABLE 2
Typical Characteristics of I^2L Gates

Parameter	Typical Characteristics at Various Injector Currents			
	I_j = 100 nA	I_j = 1 μA	I_j = 10 μA	I_j = 100 μA
Output Sink Current, I_O	300 nA	8 μA	80 μA	600 μA
Output Sat. Voltage, V_{OL}	3 mV	3 mV	4 mV	10 mV
Input Threshold	0.48 mV	0.54 mV	0.60 mV	0.66 mV
Pwr. – Delay Product (V^+ = 1V)	0.6 pJ	0.6 pJ	1.0 pJ	3 pJ
Average Prop. Delay	6 μsec	0.6 μsec	200 nsec	50 nsec
Max. Toggle Freq. (D F/F)	6 kHz	60 kHz	400 kHz	3 MHz
Input OFF Current (V_{IN} = 0)	150 nA	1.5 μA	15 μA	130 μA
Output Breakdown Voltage	3V	3V	3V	3V

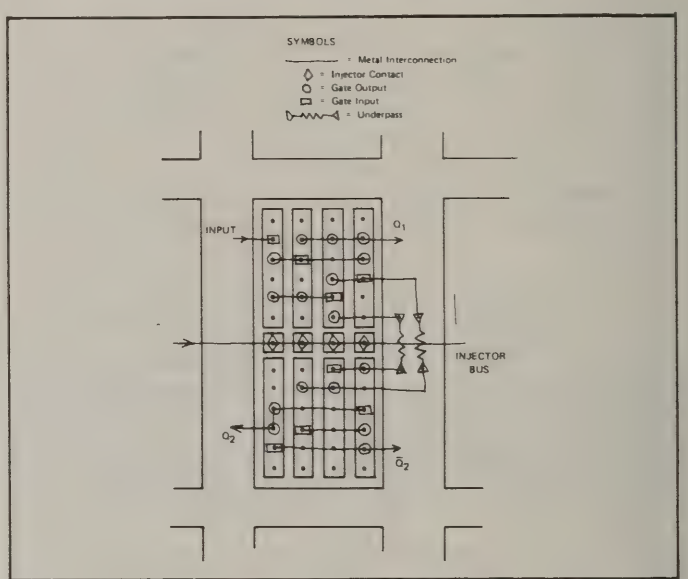


Figure 6. Sample Pencil Layout on a Logic Cell.

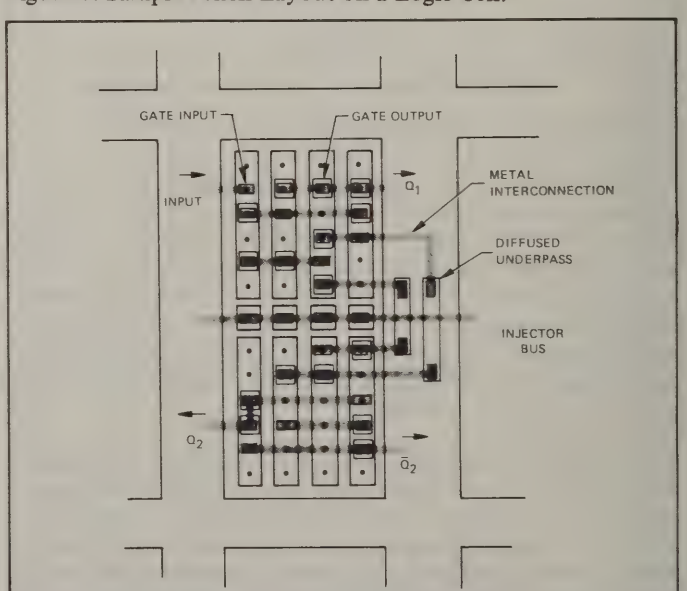


Figure 7. Sample Layout of 8-Gate Cell After Customizing it with N+ Collector Diffusion, Contact Mask and Metal Interconnection Pattern.

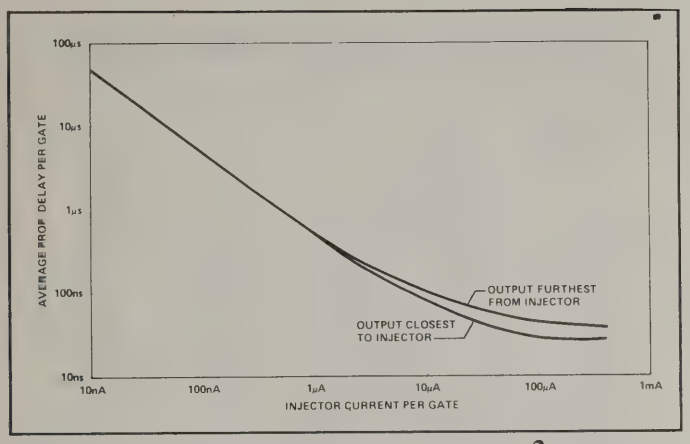


Figure 8. Propagation Delay Characteristics of I^2L Gates as a Function of Injector Current.

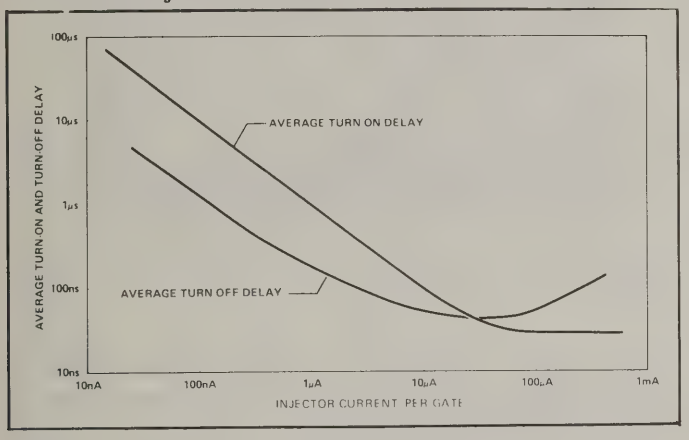


Figure 9. Average Turn-On and Turn-Off Delay vs. Injector Current.

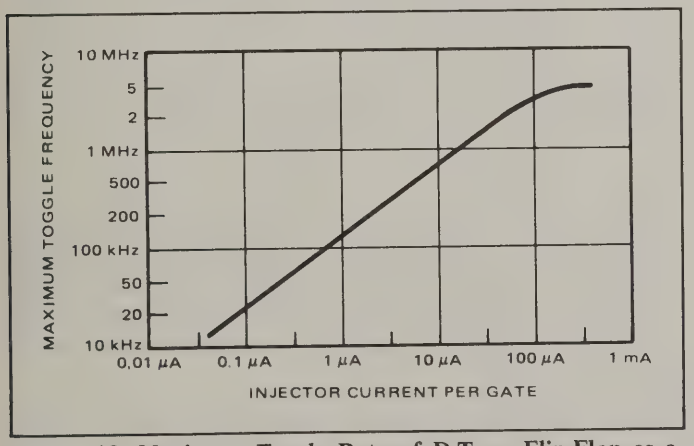


Figure 10. Maximum Toggle Rate of D-Type Flip-Flop as a Function of Injector Current.

b) Schottky-Bipolar I/O Section:

The Schottky-bipolar input/output interface sections are located along the periphery of the XR-300 and the XR-500 gate array chips. In addition, this bipolar section of the chip contains two sets of resistor arrays, located at opposite ends of the chip (see Figure 4) for programming or setting the injector current levels for the I^2L gates. By proper tapping of these resistor arrays, the injector currents of the gates can be set to any value between 1 µA to 100 µA per gate. For operating with current levels below 1 µA/gate, an external current setting resistor can also be used.

The component layout of a typical bipolar input/output interface cell is shown in Figure 11. Such an I/O interface cell contains one bonding-pad, several diffused resistors of varying values, two Schottky-clamped NPN transistors and a clamp diode to the substrate. Each of the NPN bipolar transistors are capable of sinking **10mA** of output current, with typically a saturation voltage of **0.5V**. The breakdown voltage of the bipolar output transistors is 6V; however, modified versions of the XR-300 and XR-500 I^2L gate arrays are also available with output breakdown voltage in excess of 15V. Figure 12 shows some of the most commonly used input and output interface circuit configurations available from the basic bipolar I/O cell.

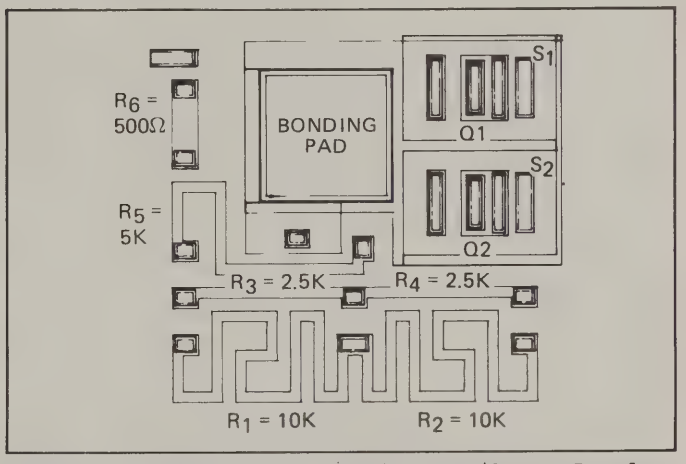


Figure 11. Typical Schottky-Bipolar Input/Output Interface Cell.

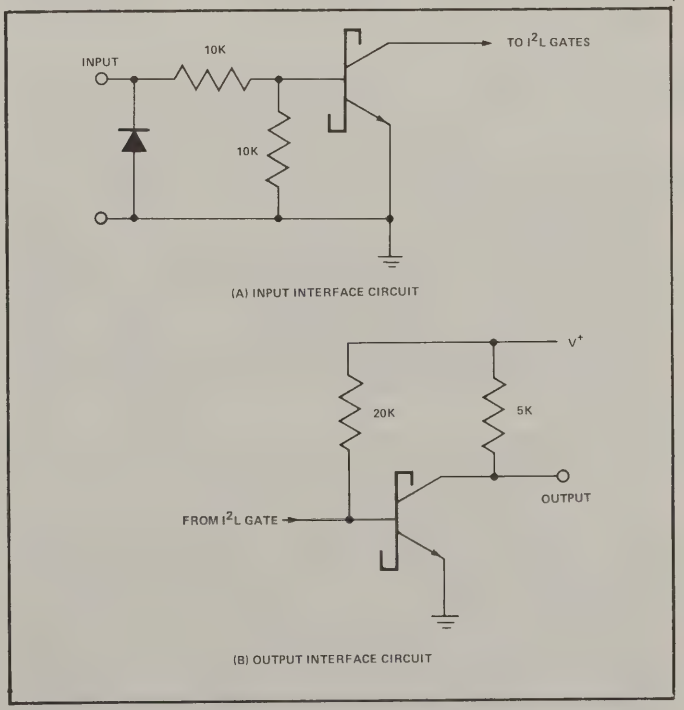


Figure 12. Typical Bipolar I/O Interface Circuits.

SEMI-CUSTOM DESIGN CYCLE

The semi-custom LSI design program utilizing the XR-300 and XR-500, is devised for maximum versatility, to suit varying customer needs or capabilities. Figure 13 gives an outline of the six basic steps associated with a typical I^2L semi-custom program. The sequence of these steps are also outlined below:

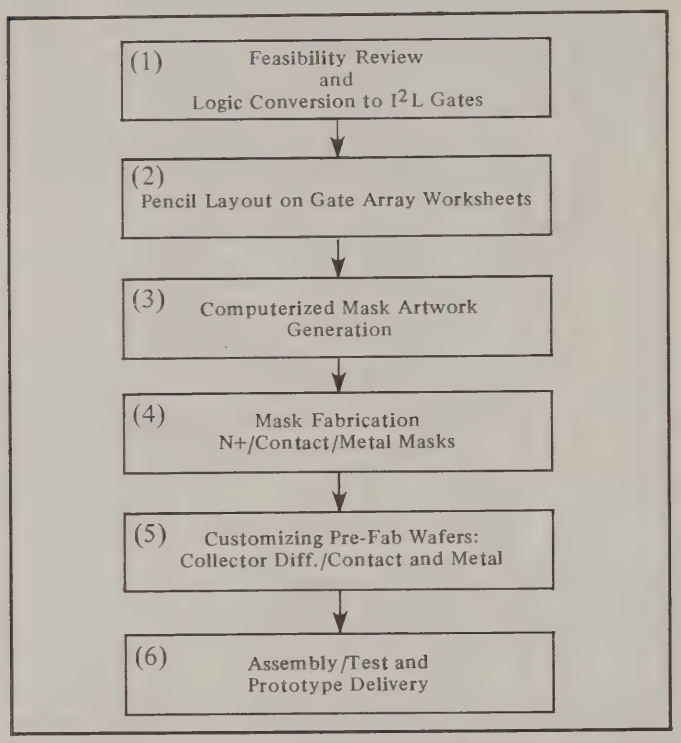


Figure 13. Sequence of Steps Associated with a Semi-Custom LSI Development Cycle.

Step 1. Feasibility Review and Logic Conversion:

Starting with the customer's logic diagram (preferably reduced to flip-flops and gates) the first step is a detailed review of the system requirements with regards to the overall gate count, I/O requirements, operating speeds, etc., to assure feasibility of integration, and to choose the most economical gate array chip to be used. If the results of this review indicate feasibility, the next step is to convert the logic diagram into I^2L gates. At this state, a computer simulation of the logic diagram may also be performed, if deemed necessary.

Step 2. Pencil Layout on Gate Array Worksheets:

Once the logic diagram is converted to I^2L gates, the next step will be to make a pencil layout of the circuit on the appropriate array worksheet. This pencil layout is done on a blank worksheet where the gate input and output locations are shown as target dots (see Figure 5). During the layout, an appropriate symbol is placed over the corresponding dot on the gate outline, and the interconnections and the underpasses between the gates are indicated by pencil lines and with the symbols defined in the layout example of Figure 6. In this layout, the bipolar I/O cells do not need to be internally interconnected. Since these cells are standardized, it is only necessary for the designer to specify if a particular I/O cell is to be used as an input or an output.

Step 3. Computerized Mask Artwork Generation:

Using a specially developed computerized mask generation technique, the three layers of necessary custom IC tooling (i.e., for custom N-type diffusion, contact window cut; and the metal interconnections) can be automatically generated by a single "digitizing" step from the pencil layout. This simultaneous and automated generation of the three custom mask layers greatly reduces the tooling cost and turnaround time, and avoids mask errors.

Step 4. Mask Fabrication:

The photographic tooling plates, or "masks," are fabricated by a pattern-generation technique from the digitized coordinate information stored in the computer.

Step 5. Customizing Prefabricated Wafers:

The prefabricated I^2L wafers containing the P-type base diffusion and the gate "fingers" (see Figure 5) are customized into completed monolithic LSI chips using the custom IC tooling generated in Steps 3 and 4.

Step 6. Assembly/Test and Prototype Delivery:

The completed monolithic chips are first evaluated on the finished IC wafer, and later assembled, electrically tested and delivered as the completed prototypes.

In many cases, the first two steps indicated in the flow chart of Figure 13, can be done by the customer, in consultation with Exar, using Exar's I^2L Design Kit and the design instruction manual. Whenever possible, such an approach is recommended, since it greatly reduces the development costs and the turnaround time.

Typical development cycle containing all the steps outlined in the flow chart of Figure 13, takes about 8 to 12 weeks, depending on the circuit complexity, and whether the customer or Exar does the logic conversion and pencil layout.

Figure 14 shows the photo-micrograph of a typical semi-custom LSI chip, fabricated using the technology outlined in this paper. As indicated in the figure, the use of 3-mask customization step results in an efficient layout and utilization of the available active devices within the I^2L gate array.

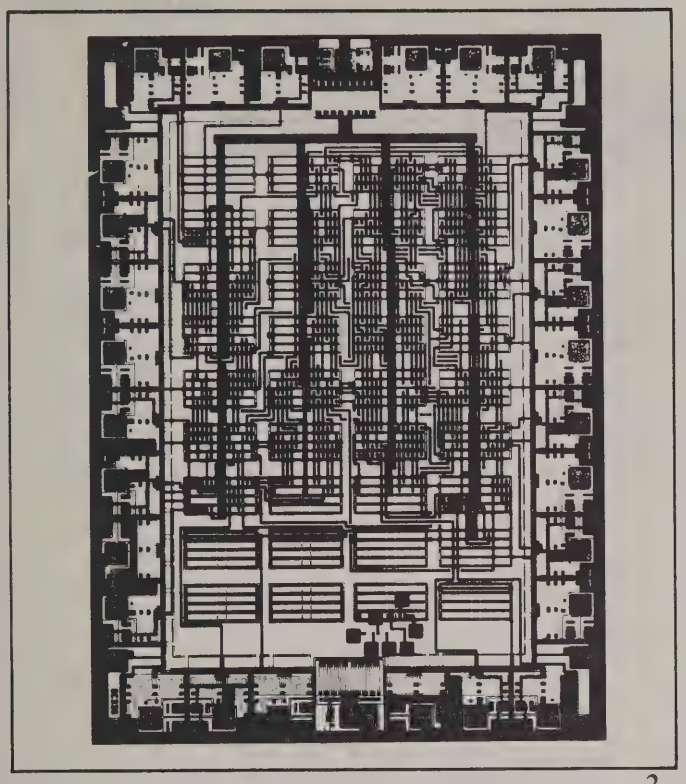


Figure 14. Photo-Micrograph of a Typical Semi-Custom I^2L LSI Chip.

ECONOMICS OF SEMI-CUSTOM DESIGN

In developing custom LSI circuits, one is confronted by the following key question: for a given production requirement, is it cheaper to develop a full or semi-custom IC? Since the performance and functional requirements of custom IC's vary greatly, there is no general answer to the above question. However, based on the overall production requirements it is possible to establish some economic guidelines for deciding which custom IC technology to use, and when.

One of the main advantages of semi-custom LSI design over conventional full custom IC development is the greatly reduced development cost. This development cost generally amounts to 10% to 30% of that required for a complete custom IC design. However, since the semi-custom design technique tends to waste some of the IC chip area due to random interconnections, the unit price of a semi-custom LSI chip in volume production is slightly higher (approximately 10% to 30%) then a full or complete custom design. Therefore, to decide which is the most economical approach, it is best to compare the estimated amortized unit cost per device for various production quantities. Figure 15 gives such a comparison for a "typical" custom LSI chip, as a function of total production requirement. The total amortized cost per unit is defined as the total cost of the development plus the production purchase, divided by the total number or quantity of units purchased. The extremely high development costs (typically in the range of $50,000 to $100,000) associated with full custom designs make the amortized unit cost of full custom IC's far more expensive than semi-custom designs, at low production quantities. Similarly, for the lower chip cost of full custom IC's make this approach more economical for high production volumes. Typical cross-over point between the economics of the full or semi-custom technology comes about in the quantity range of 50,000 pieces to 150,000 pieces, as implied by the illustration of Figure 15. However, it should be noted that Figure 15 is only a typical "case study," and that the actual cross-over point for a given program will depend on the circuit complexity, performance and test requirements, and the type of IC package used.

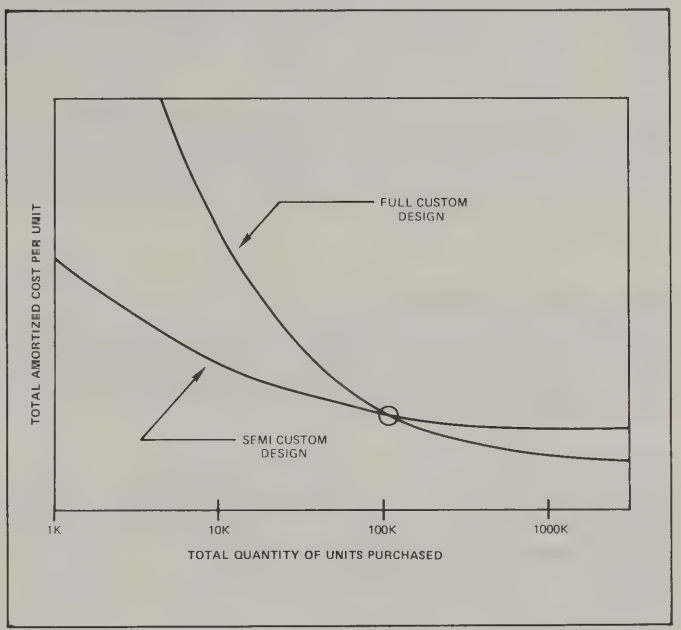


Figure 15. A Comparison of Relative Cost Advantages of Semi-Custom and Full Custom LSI Products. (NOTE: Amortized cost per unit includes the development cost.)

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

It is often possible to start a development program using the semi-custom technology, such as the I^2L gate arrays described in this paper, and later change to a full custom design when the production quantities increase beyond the cost cross-over point illustrated in Figure 15. Such two-phase approach often combines the best advantages of each of the semi- and full custom technologies. For example, the initial development can be done in a semi-custom manner, using Exar's I^2L gate arrays, and thus take full advantage of the low tooling cost and the short development cycle. As a customer's product matures and its market expands, resulting in higher volume production run rates, Exar can convert the multiple semi-custom chip approach into a single custom IC, achieving a cost reduction and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced; the IC design approach has been proven, and the design "bugs" are removed at the semi-custom stage thus eliminating the need for lengthy re-design cycles at the full custom level. Once the semi-custom chip is completely characterized in the user's system, and is used for the initial production runs, it can be gradually "phased-out" by a full custom design without interrupting the user's production line.

Application Note AN-17

XR-C409 Monolithic I^2L Test Circuit

INTRODUCTION

The XR-C409 monolithic IC is a test circuit for evaluation of speed and performance capabilities of Exar's Integrated Injection Logic (I^2L) technology. It is intended to familiarize the I^2L user and the digital system designer with some of the performance features of I^2L, such as its high-frequency capability and power-speed tradeoffs.

Figure 1 shows the package diagram of the XR-C409 I^2L test circuit. It is comprised of five separate evaluation blocks as shown in the figure. Blocks 1 and 2 are D-type flip-flops which are internally connected as frequency dividers. Each of these dividers provide buffered open-collector outputs. Blocks 3, 4, and 5 are 8-stage ring-oscillators with buffered outputs to be used for measuring gate propagation delays at different injector current levels.

FREQUENCY DIVIDER SECTION

The frequency divider sections of XR-C409 test circuits are made up of two D-type flip-flops internally connected in the (÷2) mode. These frequency dividers are operated with *serial* clocking and *parallel* reset controls.

The internal interconnections of these D-type flip-flop sections are shown in Figure 2. The corresponding package terminals are also identified in the figure. The flip-flops operate on the negative-transitions of the clock input, and reset with the reset at a "high" logic state. When the circuit is reset, all the outputs go to a "low" state. The logic polarities and the timing sequence of the circuit waveforms are given in Figure 3.

Evaluating the Frequency Divider Section

Figure 4 shows the circuit connection for the frequency divider section of the XR-C409. The recommended clock input level is 0V and +1V for the "low" and "high" levels. For optimizing high frequency performance, a square wave clock input is recommended with a source impedance $\leq 100\Omega$.

Biasing of Injectors

All of the 16 I^2L gates forming the frequency divider sections are biased by the total injector current, I_T, applied to the injector terminal (Pin 1) as shown in Figure 4. The total injector current, I_T, applied to the flip-flop sections of XR-C409 is set by the external bias resistor, R_B, as:

$$I_T = \frac{V^+ - V_{be}}{R_B} \qquad (1)$$

where V_{be} ($\approx$0.7V) is the transistor base-emitter voltage drop.

The total injector current ,I_T, is shared amoung 16 individual I^2L gates forming the frequency-divider sections. Thus, the operating current of each gate, I_j, is equal to 1/16 of the total injector bias, or:

$$I_j = I_T/16 \qquad (2)$$

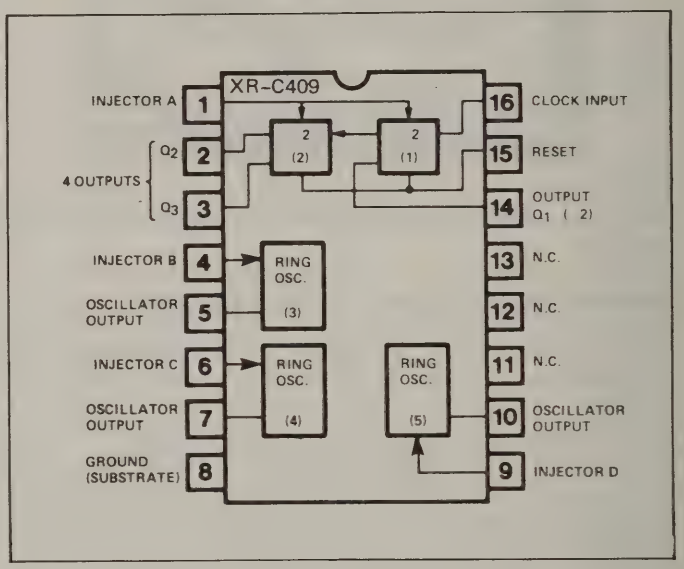


Figure 1. Package Terminals for XR-C409 Test IC.

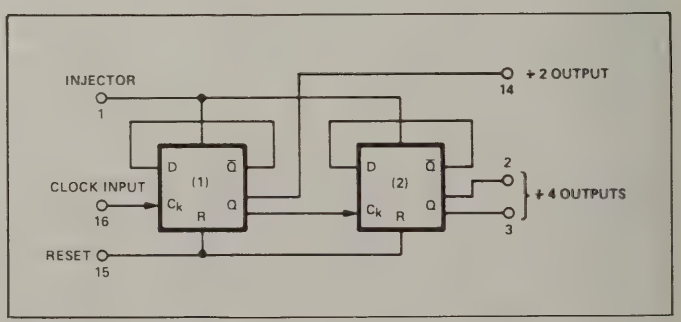


Figure 2. Block Diagram of Frequency Divider Section.

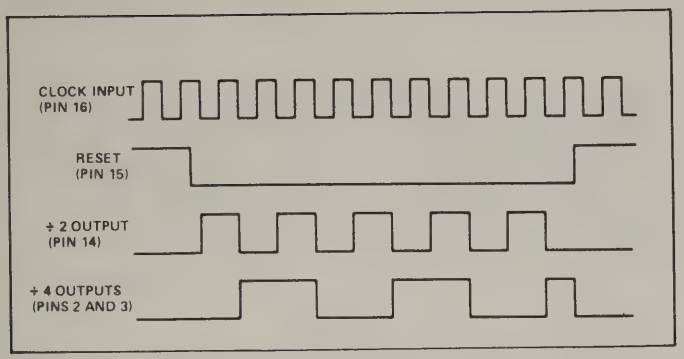


Figure 3. Timing Diagram for Frequency Divider Section.

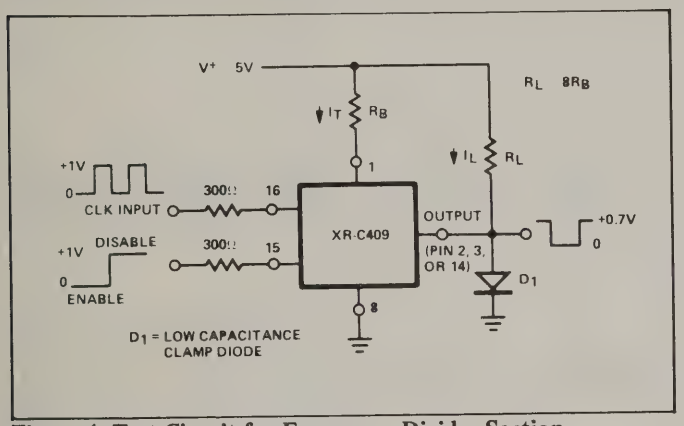


Figure 4. Test Circuit for Frequency Divider Section.

Measuring Output Waveforms

Each of the output terminals of XR-C409 frequency-divider are open-collector type terminals which require a pull-up resistor to positive supply voltage. Thus, the output rise-time is limited by the external RC time constant due to the load resistance, R_L, and the parasitic and/or load capacitance, C_L.

Figure 5 shows a recommended circuit connection to test the output swing at high frequencies, using a low-capacitance clamp-diode, D_1, to clamp the output swing to ≈+0.7V above ground.

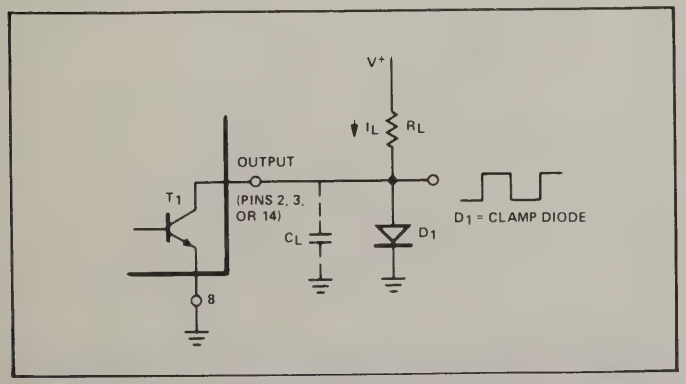


Figure 5. Recommended External Connections to Measure Output Waveforms.

The value of the load resistor, R_L, is determined by the current sinking capability of the output transistor, T_1, internal to the chip. Since T_1 is the output of an I^2L gate, its worst case sinking current is limited to the individual gate current, i.e.:

$$I_L \leqslant I_j = \frac{I_T}{16} \qquad (3)$$

This current-sinking capability in turn limits the minimum value of load resistance R_L to:

$$R_L \geqslant 16\ R_B \qquad (4)$$

The peak output swing is limited to approximately 3 volts due to the collector-base breakdown of the I^2L gate output, i.e., transistor T_1 of Figure 5.

High Frequency Capability

The maximum operating frequency of I^2L frequency-divider circuits is a function of the total injector current. For low-current operation, the maximum toggle-frequency of the flip-flops forming the frequency-divider section increases

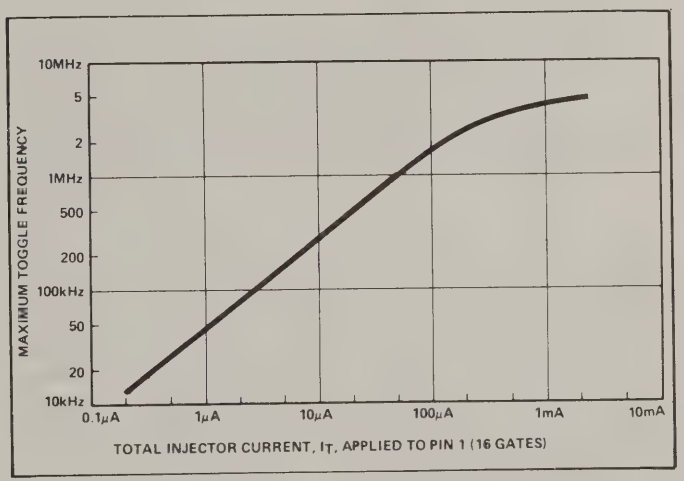


Figure 6. Typical Maximum Toggle Frequency vs. Injector Current Characteristics for XR-C409 Frequency Divider Section.

(NOTE: Clock Input: $1V_{p\text{-}p}$ Square Wave)

linearly with increasing injector current. Typical maximum toggle frequency vs. injector current characteristics are shown in Figure 6. Note that the maximum toggle-rate obtainable is in the range of 3 to 5 MHz, at a total injector current level of 1 to 2 mA, which corresponds to individual injector currents of approximately 60μA to 120μA per gate.

RING-OSCILLATOR SECTIONS

The ring-oscillator sections of XR-C409 test circuit are intended for measurement of propagation delays associated with I^2L gates. Each of these oscillators are made up of a cascade of 8 four-output I^2L gates. Figure 7(a) shows the basic electrical equivalent circuit of a four-output I^2L gate. Its corresponding logic symbol is shown in Figure 7(b). The basic gate operates as an inverter with single input and four outputs.

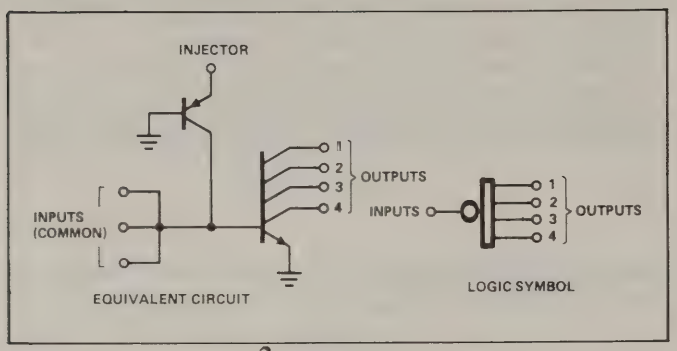


Figure 7. Four-Output I^2L Gate.

The propagation delay through an I^2L gate depends on the following sets of parameters:

1. **Device design:** (i.e., manufacturing methods and device layout used in fabrication process).

2. **Injector current level:** (gate switching speed increases with increasing current, until a maximum is reached).

3. **Choice of outputs used:** (the output closest to the injector has minimum propagation delay at high currents).

4. **Number of outputs used:** (if fewer outputs are used and the unused outputs left open, the gate delay is Lower at low currents. However, at high currents, i.e., $I_j \geq 100\mu A$/gate, gates with fewer outputs left unused show lower delays. This is due to excess storage-time effects due to open-circuited gate outputs. See Figure 10.)

Figure 8 shows the basic seven-stage ring-oscillator circuits included on the XR-C409 chip to evaluate the propagation delay characteristics of I^2L gates. Since the delay characteristics depend on the choice and the number of gate outputs used, the test IC includes three separate ring oscillator sections. The ring oscillator of Figure 8(a) corresponds to section (3) in the package diagram of XR-C409 shown in Figure 1. This oscillator uses only one gate-output per gate. The output used is the one closest to the injector, with the remaining outputs left open-circuited.

The ring-oscillator of Figure 8(b) uses two gate outputs per stage. The outputs used are the two closest to the injector. The ring oscillator of Figure 8(c) has all four outputs shorted together.

All three oscillator sections of XR-C409 have *separate* injectors, but share a common ground (pin 8). Each oscillator also has a separate output buffer stage.

Figure 9 shows a recommended test circuit for evaluating gate delay vs. gate current characteristics using the ring oscillator sections of XR-C409. Since each ring-oscillator section is comprised of 8 gates, the actual injector current per gate, I_j, is 1/8 of the total injector current, I_T,:

$$I_j = \text{injector current/gate} = \frac{I_T}{8} \qquad (5)$$

The total injector current, I_T, is determined by the external bias resistor, R_B, as given by equation (1).

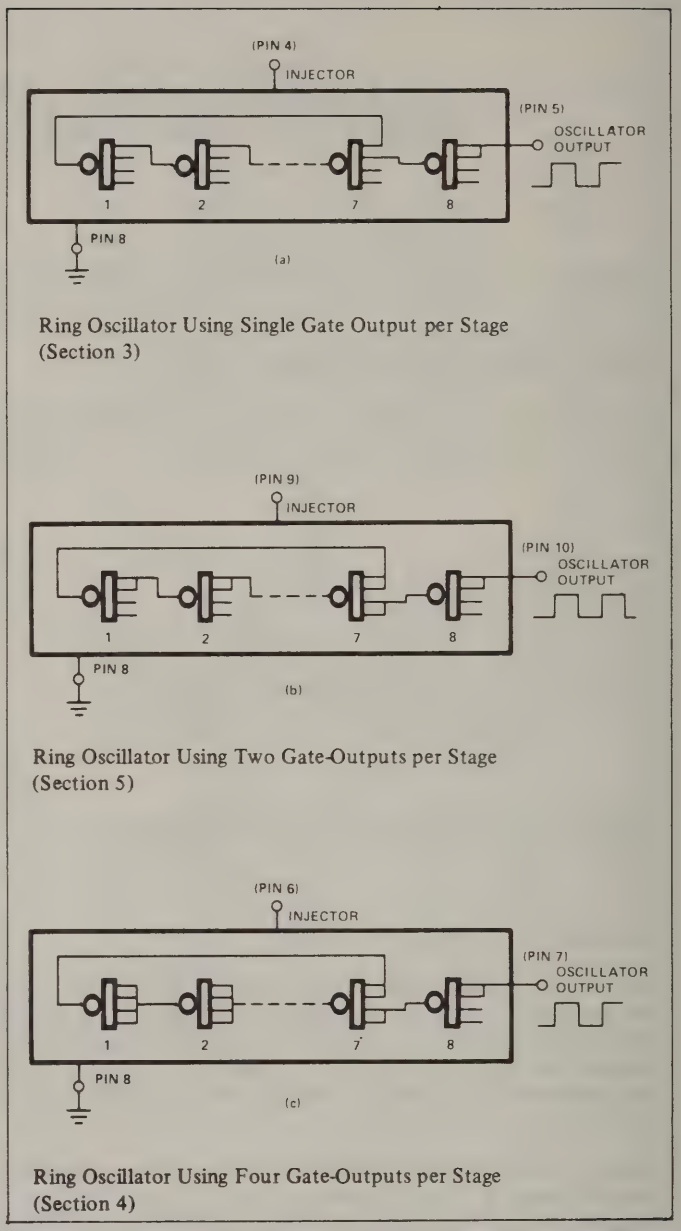


Figure 8. Equivalent Circuits of the 7-Stage Ring Oscillator Section.

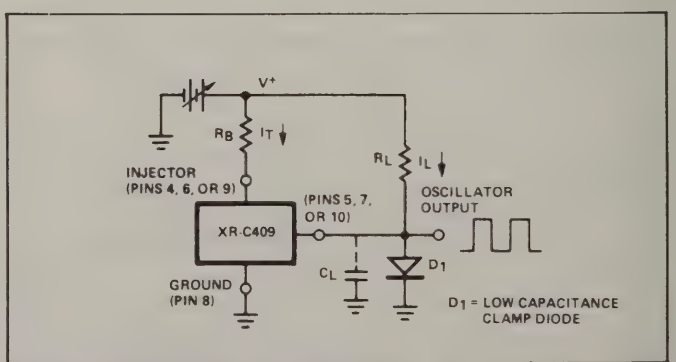


Figure 9. Recommended Test Circuit for Evaluating Power-Delay Characteristics of I^2L Gates Using Ring Oscillator Sections of XR-C409.

Measuring Output Waveforms

The output terminals of XR-C409 ring counter sections are open-collector type terminals, similar to the outputs of the frequency divider sections. Thus, the outputs require pull-up resistors to the positive supply voltage. The output rise-time is strongly affected by the external RC time constant due to the load resistance, R_L, and the parasitic load capacitance, C_L. In the test circuit of Figure 9, a low-capacitance clamp diode, D_1 is used to limit the output swing and thus minimize the slow rise-time effects.

The minimum value of load resistance, R_L, is determined by the current sinking capability of the output I^2L gate. For proper operation of the ring-oscillator circuits, the load current, I_L, should be limited to:

$$I_L \leq \frac{I_T}{4} \qquad (6)$$

which limits the output load resistance, R_L, for ring-oscillator sections to:

$$R_L \geq 4\,R_B \qquad (7)$$

Calculating Propagation Delays

The average propagation delay τ_d per gate can be calculated from the ring oscillator frequency, f_o as:

$$\tau_d = \frac{1}{2Nf_o} \text{ sec} \qquad (8)$$

where N is the number of stages in the ring oscillator.

For the case of the 7-stage oscillator circuits in the XR-C409 test chip, τ_d can be calculated from equation (8) by setting N = 7.

Figure 10 shows the typical gate-delay vs. injector current characteristics measured from the three ring-oscillator sections of XR-C409. In the figure, the gate delay is plotted as a function of the injector current per gate. The gate geometry layout of XR-C409 ring-oscillator sections is not optimized for high frequency operation.

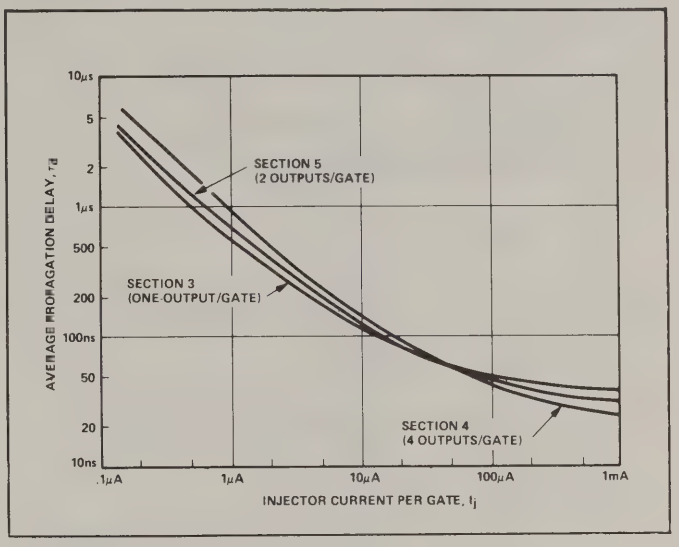


Figure 10. Typical Propagation Delay vs. Injector Current Characteristics as Measured from 7-Stage Ring Oscillator Section of XR-C409.

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The quality assurance program at Exar Integrated Systems defines and establishes standards and controls on manufacturing, and audits product quality at critical points during manufacturing. The accompanying Manufacturing/QA process flows illustrate where quality assurance audits, by inspection or test, the manufacturing process. The insertion of these quality assurance points is designed to insure the highest quality standards are maintained on Exar product during its manufacture.

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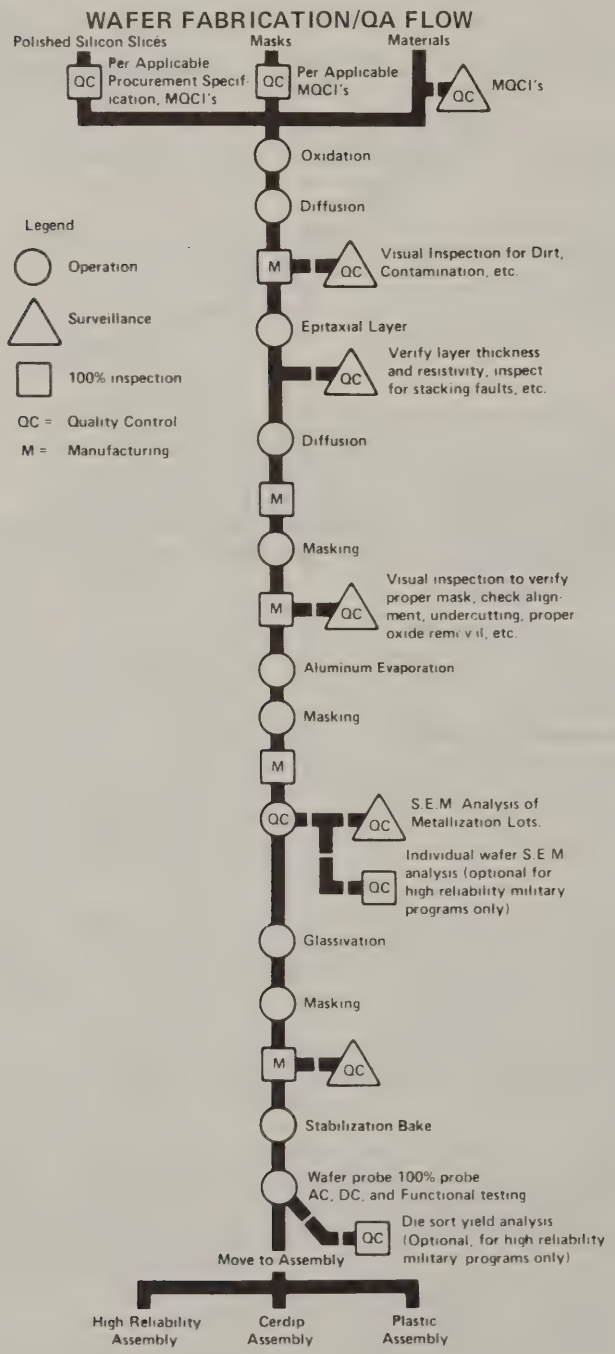

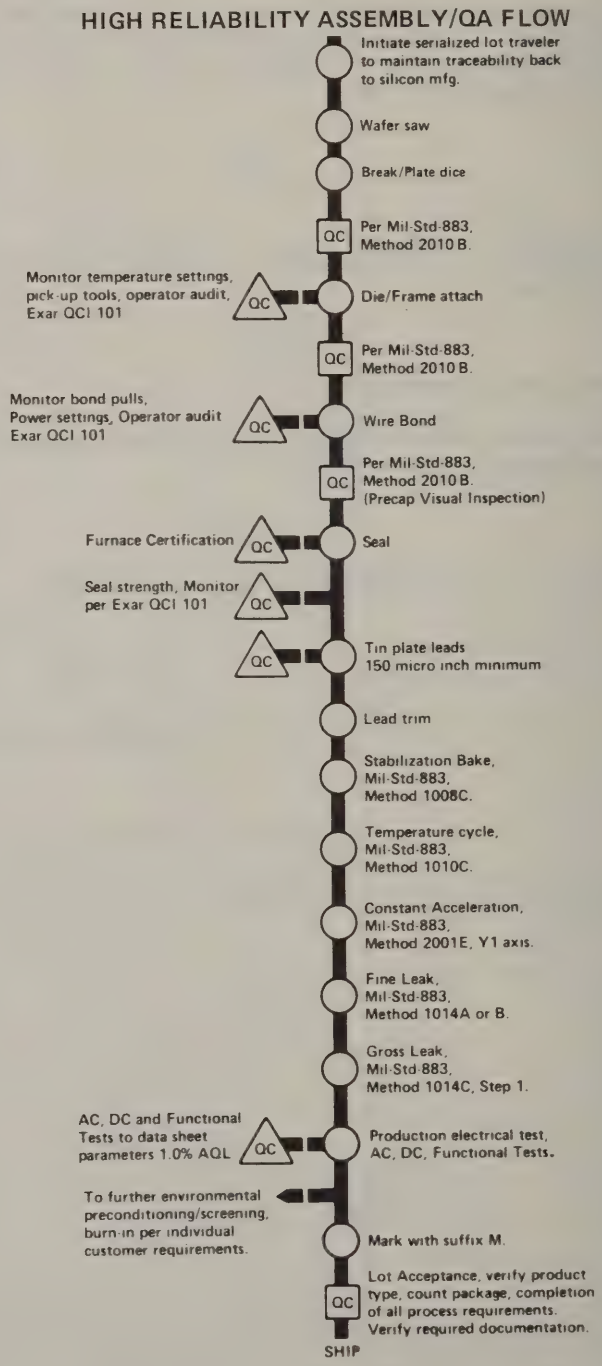

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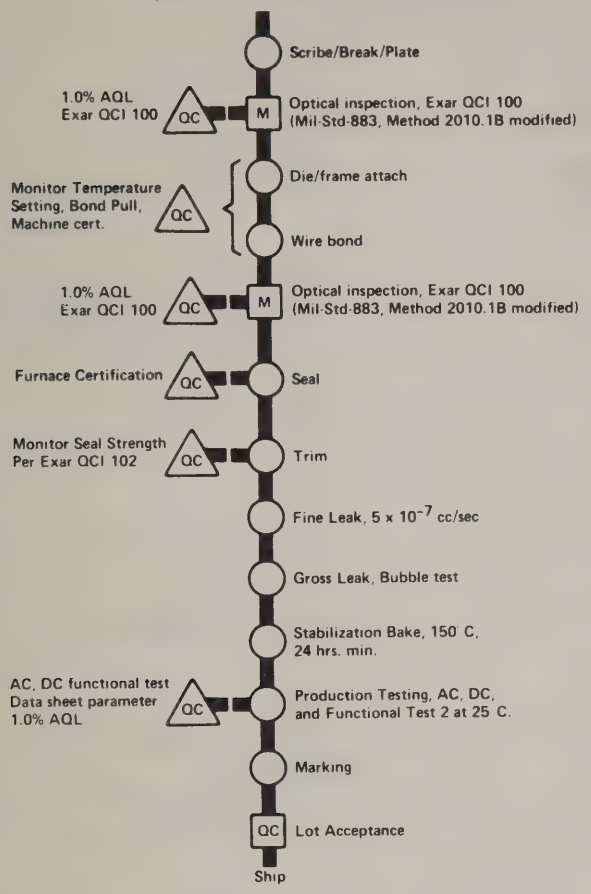

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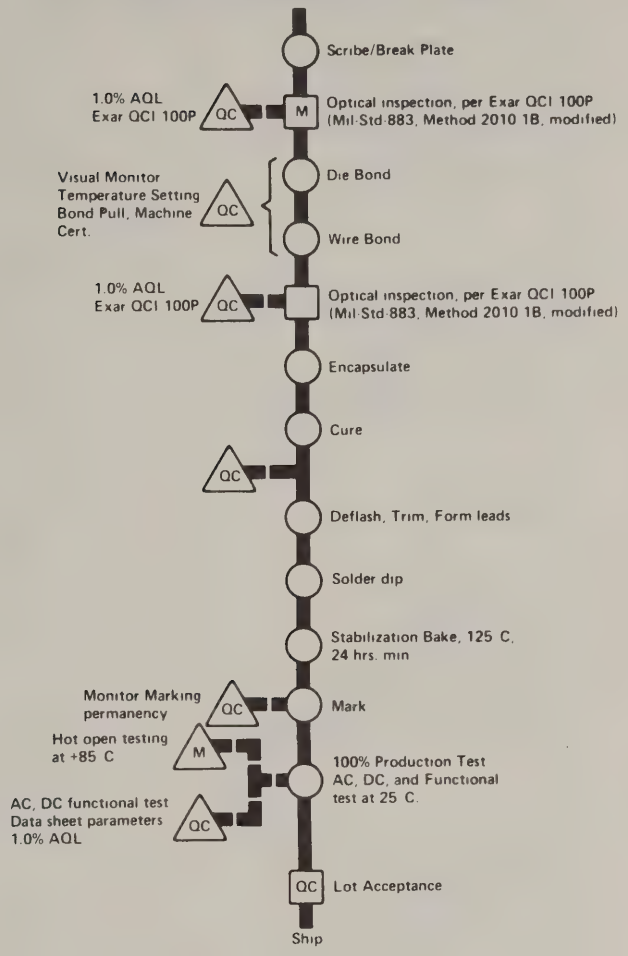

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Example:

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APPLICATIONS DATA BOOK:

This book contains a complete and up-to-date set of application notes prepared by Exar's technical staff. These application notes cover a wide range of subjects such as FSK modems, active filters, telecommunication circuits, electronic music synthesis and many more. In each case, specific design examples are given to demonstrate the applications discussed. (70 pages)

FUNCTION GENERATOR DATA BOOK:

This comprehensive data book contains a number of technical articles and application notes on monolithic voltage-controlled oscillators (VCO) and function generator IC products. In addition, the data sheets and technical specifications of Exar's monolithic VCO's and function generators are given. (50 pages)

LINEAR AND DIGITAL SEMI-CUSTOM DESIGN BROCHURE:

This brochure contains a detailed description of Exar's unique bipolar and integrated injection logic (I^2L) semi-custom design technology. Economic advantages of the semi-custom designs are discussed and economic guidelines are given for choosing the most cost-effective solution to a custom IC requirement. In addition, this brochure provides technical information on Exar's Master Chips and IC Design Kits. (36 pages)

OPERATIONAL AMPLIFIER DATA BOOK:

This book contains a collection of technical articles on the fundamentals of monolithic IC op amps. Some of the basic op amp circuits are given and the application of IC op amps in active filter design are discussed. The book also contains a complete set of electrical specifications in Exar's bipolar and BIFET op amp products. (60 pages)

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